SILICON AND GERMANIUM VAPOR-LIQUID-SOLID WIRE MATERIAL PROPERTIES AND DEVICES

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Semiconductor vapor-liquid-solid wires have been grown for over 48 years and remain a topic of active interest today. In my doctoral research I synthesized silicon and germanium wires via the vapor-liquid-solid method, studied their material properties and applied them to systems. The main application targeted was photovoltaic cells. Synthesis methods were developed and optimized to create materials suitable in principle for this engineering goal. Photovoltaic cells were constructed and their performance measured. Material properties of the vapor-liquid-solid materials were measured to obtain the needed parameters to further understand the design and practical limits of photovoltaic cells constructed from the materials. In addition to photovoltaics vapor-liquid-solid wires were employed as scanned probes. Properties unique to vapor-liquid-solid synthesis were used to create probes en-masse that would be difficult or costly to fabricate by other means.

BIOGRAPHICAL SKETCH

Brian A. Bryce was born on January 10, 1983 at George Washington Hospital in Washington, DC to Robert and Pamela Bryce. His long term interests became clear early. While in Elementary school he received his first camera from his grandfather on his father's side, Glenn, a 126 instamatic. His grandfather on his mother's side, Bill, gave the family their first computer, a Commodore 64, on which Brian wrote his first programs in BASIC following instruction by his brother Glenn. At the age of 8 Brian was hit by a car crossing a street and broke his femur. Fearing brain damage he was taken by helicopter to Children's Hospital in Washington, DC where he was placed in intensive care. He was put in traction with a bolt through his leg and placed on a morphine drip. This experience shaped his future attitudes toward drugs including his opposition to alcohol use. After a full body cast he went through physical therapy and learned to walk again. Two years later he was among the fastest runners in his class. By this time he was very interested in video games and through them computers. His experimental learning badly fragmented the hard drive of his father's 286 which was purchased to write his definitive biography of Frederick A. Cook. This incident resulted in a ban on computer use save for school work, and made computers that much more appealing. At the end of middle school he got his first computer of his own a 350 MHz Pentium II as a gift from his parents. In high school he continued his interest in photography purchasing his first SLR, a Canon AE-1 Program. In high school Brian ran cross country and played on the equivalent of the quiz bowl team. His team won the state cross country championship twice. He also took advanced classes focusing on science, history and programming. Upon graduation he enrolled at University of Maryland, College Park. He debated majoring in History or Electrical En-

gineering. Pragmatism won and he chose Electrical Engineering to learn how to design computer processors. In his second year he began research in Bruce Kane's Quantum Computing group under the guidance of PhD candidate Kenton Brown from whom he learned many valuable scientific skills. Unable to understand the theory motivating this research and disappointed with the missing physical fundamentals in the Electrical Engineering courses, he added a Physics major to his work. Also in his second year of college at age 20 he was diagnosed with cancer, malignant melanoma. Returning to the hospital complex where he was at 8, this time Washington Hospital Center, he had surgery during spring break so as not to disrupt his course work. The summer following surgery he completed a solo coast to coast camping trip following in the footsteps of previous long family camping trips. Two and half years later he graduated from Maryland with degrees and honors in Physics and Electrical Engineering. He traveled to New Zealand after graduation for more photography, and hiking before moving to Ithaca, NY to attend Cornell University. He spent his first year as a teaching assistant and in his second joined Professor Tiwari's group to pursue research in vapor-liquid-solid wires and devices. During his graduate school work he started a small company, teho Labs to try his hand at entrepreneurship. After graduation he will begin working at IBM Research in Yorktown Heights, NY researching a new type of transistor.

To the forgotten multitude who have fallen bringing light to where there once was none.

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CHAPTER 1

INTRODUCTION

1.1 Overview

This thesis is organized primarily topically and secondarily chronologically. The topics are generally arranged in the order the research was started. This is done to convey how one area led to the study of other areas. I have tried to note in the manuscript where topical organization has obfuscated the reason for some work remarking on where the result will become relevant later in the thesis.

The principle theme of my thesis research was the application of vapor-liquid-solid wires to photovoltaics. For three of the five years this thesis represents this was the sole focus of my research. In the last two years scanned probes became an additional theme with the photovoltaic work continuing.

The body of this chapter discusses the general historic, economic, and social context for photovoltaics and more broadly energy. The reader purely interested in scientific discussion and results may choose to skip sections of this material without loss of continuity. This material provides the motivation for undertaking the research.

The second chapter of this thesis gives the needed background to understand vapor-liquid-solid (VLS) synthesis. It also presents results of the synthesis methods that were employed to create the materials for the rest of the chapters of the thesis. It is largely designed to give the reader intuition on how to create the needed VLS materials and explain the difficulties that exist in achieving certain results.

The third chapter of this thesis presents a transmission electron microscopy based study of germanium wires grown on titanium using gold as the catalyst. It studies this system through the use of a specially created sample preparation technique.

The fourth chapter of this thesis discusses the results of VLS wire photovoltaics both in theory and in practice. It presents the measured performance of VLS photovoltaic cells and discusses the problems encountered creating this type of solar cell.

The fifth chapter of this thesis examines the fundamental material quality of the VLS materials grown via measurements of carrier lifetimes. It compares Al and Au catalysts and examines the diameter dependence of the lifetimes observed.

The sixth chapter of this thesis explores the use of VLS grown materials as high aspect ratio atomic force microscopy probes. It explores the advantages and limitations of these probes by imaging high aspect ratio structures. These results are compared with results for commercially available probes.

The appendices discuss additional experimental methods that would be of interest to persons wishing to repeat or extend the methods used in the main chapters of the thesis.

1.2 Is there an energy problem?

The general consensus of society at the time of writing this document is that there is an energy problem. However the answer to if there is actually an energy

problem is more complex than it might seem. Human energy consumption is a function of how the humans in question choose to live, so the idea of there being a problem or not is a value judgment, as such it cannot be made completely objective. These societal expectations are critical to both knowing if there is a problem and to knowing if the solution to a problem has been found.

Ignoring economics, for instance, one could easily argue that humanity today has the means to create vastly more energy than it currently uses. Problem solved? With society's cooperation it maybe, but not without it. There are also even larger questions that should be considered beyond what society wants today and what is technically achievable. These questions are beyond my formal expertise, but I have spent many years thinking about them and so a discussion of these ancillary issues and motivations is worthwhile. The rest of this chapter explores these issues, and I hope prompts further thought on the subjects introduced. Research is always conducted in some social context; energy research in particular can be tangled easily with non-objective things as diverse as politics and religious beliefs.

1.3 Finite resources

All life regardless of type has an inbuilt drive or mechanisms to propagate itself maximally; life without this drive is simply outcompeted for resources [1]. Humanity is no different. Like any species in an environment there is some carrying capacity of the environment for the species. The particular needs of a species determine what the value of this carrying capacity is. In evolutionary terms modification of this limit is generally fairly fixed with species adapting

slowly to outdo each other. Humanity is an exception to this rule in that our primary adaptation is being adaptable. Most of our behavior is learned and rather than having claws we construct knives and when a knife is not appropriate we construct something else. Other species also use tools but humanity uses the most tools. These tools combined with social expectation for behavior and quality of life significantly modify what the carrying capacity for humanity is at any time.

History can be viewed as the story of humanity struggling to increase its carrying capacity. This is not a uniform process. When intraspecies pressures reach a critical point war is often the result, diseases also have been highly disruptive historically changing the structure of society and our environmental interactions. However the most common solution to competition is to adapt society or invent a new tool. When a new tool or behavior is highly disruptive to society we deem it a revolution. Most tools and behavior changes are gradual and can be viewed as the evolution of humanity as a collective organism similar but hierarchically different from eusocial superorganisms [2]. However, occasionally a revolution will occur. Most revolutions, technological or otherwise, have the net effect of increasing human carrying capacity and relieving intraspecies pressures. The most clear example of this is the founding of civilization itself. This was enabled by the invention of sedentary agriculture. Of course one day someone did not decide they would settle down and plant domesticated wheat, that process was slow. What was not slow was the organization of labor to build irrigation on a large scale and the spread of the knowledge of how to do this once one area in a region had achieved this.

Today many of those who are concerned about environmental effects in the

context of the energy problem often look back to preindustrial society as a time of harmony with nature. However really one must at least look back to before the Egyptian, Mesopotamian, Indus and countless other civilizations to see a time when humanity had not reached its natural carrying capacity, even then the line is a blurry one. Since the founding of civilization humanity has been consistently modifying our environment and shifting more and more labor to the arts, including science that enable higher and higher carrying capacities via technological and social innovations. This includes nation states and the steam engine, the book and the Haber-Bosch process, money and penicillin.

Each of these innovations has had a profound effect on society and through its organization on how many people our planet can support. In the end however the planet is finite. It certainly can be argued that we are nowhere near the physical limit yet, but what is true is that no matter what hurdle is removed there will be another and it should be asked if the better solution to intraspecies pressure is a tool or a social contract. It also should be asked if the present problem or the next problem is less intrusive.

1.4 Patch or reform

The symbol of the energy issues society faces today is often the automobile, even though in the United States the transportation sector uses only about 28% of all energy [3]. This is largely because individuals interact through filling stations directly with the price of this energy on a regular basis. For this reason it is often the focus for political purposes, with the ringing cry that we must increase fuel efficiency of vehicles. Superficially this seems like an excellent solution to this

energy consumption issue. However like the photovoltaic research that is the topic of most of this thesis making a car is not a simple confined system and using a car certainly is not. Adding technology is a patch or additive solution. Additive solutions always cost more than reform solutions which are harder for society to accomplish because individuals generally are resistant to personal behavior changes.

To illustrate this in the car case consider two options: we could double the fuel efficiency of all transportation through technology or everyone could live twice as close to work. The net fuel consumption would be the same but the later would require less expensive systems. Cost is generally a proxy for environmental impact when distortions of labor and market subsidy are removed. If you live close enough to everything you need you can walk! This simple argument makes it clear that from the environmental perspective the harder social change is probably better.

However we should also consider the other option, perhaps it is almost as good. Let's say we double fuel efficiency, will we half our emissions? It is actually not likely. What might be more likely is that that cost savings will be used to allow for a longer commute where housing might be less expensive, thus just as much fuel might be used. Perhaps such a solution would simply increase sprawl. Or perhaps society will become more aware of the constraint and learn new behaviors which are retained when the new tool becomes available. What is probably true however is if a solution is developed before social behavior adapts that society may use the solution in an unintended way.

1.5 The cost of energy

Different forms of energy cost different amounts, and there is no simple way to actually calculate the cost of the environmental effects. The ongoing monetary cost of hydropower from a large project may be quite low as the cost of the plant has long been amortized. However, these projects disrupt aquatic animal migrations, and prevent natural fertilization via flooding (the dams on the Columbia River come to mind in the former case, and the Aswan High Dam in the latter case). Coal mining regularly takes human lives, how can you possibly price that? The tons of carbon put in the atmosphere is also hard to price.

My general observation has been if the environmental impact is not localized and thus does not affect local people's lives they are willing to pay very little for it. Ithaca is a great example of this. Currently hydrologic fracturing is enabling the extraction of natural gas from the Marcellus shale. Generally speaking Ithaca residents strongly oppose this form of mining, largely on environmental grounds. These environmental issues include fear of local water contamination and climate change concerns. From a climate perspective natural gas is better than coal in energy vs. carbon output. For this reason Cornell switched its combined heat and power plant to natural gas [4]. However Ithaca's primary power plant is still AES Cayuga, a coal fired plant in Lansing, NY on Cayuga Lake. Activists against hydraulic fracturing claim they care about climate change, if that is true then logically excluding water issues they should be in favor of as much natural gas extraction as possible to displace as many coal plants as possible. They also should be fighting for the closure or refitting of AES Cayuga, even excluding the human cost of coal mining. Because they generally are not it is safe to conclude the primary reason motivating

the opposition is fear of a local environmental impact that could affect them directly. Most of these Ithaca residents are happy to shift environmental costs elsewhere to less wealthy countries and communities, with little reduction in their hydrocarbon use.

This is a natural human tendency. Even in highly educated areas such as Ithaca local self-interest appears to trump global best interests. Adam Smith's observations [5] would appear to hold, modified only in that the environmental values of the individuals affect their internal pricing structure if the environmental impact is known acutely.

Given this reality the energy problem in the context of climate is really an economic problem. It is both what the market will bear in terms of cost for energy and what local price communities are willing to pay environmentally to profit from resource extraction. Regional and global impacts are very hard because definitionally the impact cannot be priced internally by the independent person even when they have "good" social values. The Chesapeake Bay watershed is a very nice and somewhat local regional example of this. It extends all the way to southern New York including the local communities of Corning and Binghamton. Generally speaking these communities do not think of crab fisherman in Maryland when they think of what goes into the Susquehanna and its tributaries. This combined with the lack of a regional structure (inside a *single* nation state) to price the effects at a distance has impeded the health of the Chesapeake Bay for decades.

As noted, economics of the community determines both the environmental and market costs of energy. If the global impact of potential anthropogenic climate change is to be addressed this means either global values have to be

established so that all communities price this impact or alternatives must exist that can compete on a purely monetary basis with fossil fuels. If they do not fossil fuel use will continue simply shifting where it is burned. It is very much like the car example earlier. Even if reform is taken locally in one country, the decrease in demand will lower prices and increase use somewhere else. Given the geopolitical impossibility of uniform regulation and values it would seem the only option is to invent a technology that is better on a purely monetary basis and let the market adopt it automatically. This is stunningly difficult considering the cost of producing a barrel of oil from an established field in Saudi Arabia is only 2-3 dollars [6]. A barrel of oil equivalent is about 1.7 MWh [7].

1.6 Photovoltaics and the energy problem

The metric of a dollar a watt is often floated as a magic number for photovoltaics. Saudi oil costs about 1.8 dollars per MWh. If a solar installation lasts for 30 years, even at 12 hours of perfect efficiency 365 days a year, that amounts to 7.6 dollars per MWh a 422% increase. This estimate is wildly optimistic. Energy markets are sensitive to a few percent change in pricing. Thankfully from a climate perspective Saudi oil is one of the cheapest sources of hydrocarbons on the planet. Certainly oil is priced far in excess of 3 dollars a barrel. Nevertheless this extraordinarily low cost brings up an important point for photovoltaics in the market place, and that is balance of system costs.

Even if the photovoltaic cells are free there are still costs related to installing the cells. These are wiring, inverters, mounting, labor and others referred to collectively as balance of system costs (BoS). The 1 dollar/Watt goal quoted above

includes these costs. In 2010 BoS costs were 1.48 dollars/Watt and cell costs were 1.78 dollars/Watt [8]. There is room for improvement in both but what is equally true is the 25 cent per watt photovoltaic energy that would prevent the cheapest sources of hydrocarbons from being used is likely not technically achievable ever and certainly not in the near term.

However, this does not mean photovoltaics and solar in general do not have an important place, particularly if society can be mobilized to price the benefit of non-fossil forms of energy. In this context what is more important perhaps is that photovoltaics succeed in other metrics.

The most important such metric is certainly energy gain. Simply because a system produces energy at a low cost does not mean it has energy gain. The price differential between the cheapest forms of fossil energy (such as coal) in one area of the world can be used to create a more portable form of energy that may not have energy gain but is worth more to a distant market. This certainly occurs regularly. Thankfully this is not true of conventional photovoltaics. Energy gains of current marketed photovoltaics have been estimated to be on the order of 10 in a detailed study that attempted to include all costs of the system over their lifespan, including plant costs [9].

With energy gain the energy problem is solved in principle as there is a lot of solar energy available. In practice however photovoltaics face other challenges. Being intermittent sources of energy storage is a major issue if a significant percentage of total energy is to come from such a source. In the jargon of the power industry this makes intermittent renewables unsuitable currently for base load.

Solar has an excellent public image in terms of environmental impact how-

ever solar is not environmental impact free. Raw material extraction for manufacture clearly has an impact as does the install footprint of the cells which displaces local habitat. The second of these impacts generally benefits from high efficiency solar cells which have smaller footprints for constant power. High efficiency cells also reduce BoS costs. For these reasons cell efficiency has been the major focus and metric used by the solar community. Energy gain however may be more important, though cost per watt is generally correlated to energy gain and may often be used as a proxy for such gain. Thankfully studies of the total system including manufacturing and end of life are increasingly taken into account in planning research priorities [10].

1.7 Summary

Taken in total photovoltaic performance improvements appear beneficial and warrant continued investment and research. This observation however is not a simple one as production of any form of energy is complex and complete cost and impact estimates are hard to make. This picture is further complicated by social and political issues and market distortions both via intentional subsidy and lack of a pricing mechanism (e.g. global carbon).

CHAPTER 2

VAPOR-LIQUID-SOLID WIRES AND THEIR SYNTHESIS

2.1 Introduction

The vapor-liquid-solid (VLS) method of growing semiconductor crystals was described by Wagner and Ellis in 1964 [11]. In the last 48 years thousands of papers have been published both studying the method itself and utilizing it for the creation of systems. In spite of 48 years of intense study VLS remains an active area of study today. The VLS mechanism is in some ways very complex and from a material science perspective there remains much to learn, particularly in the case of VLS with less commonly used catalysts. There have been several good review papers [12] [13] written on VLS semiconductor wires and the VLS mechanism therefore here I do not wish to write yet another review on the topic but rather give a simple but useful picture of how VLS works before covering growth experiments that were necessary to support the rest of the work in this thesis.

2.2 Vapor-liquid-solid growth in theory

As the name implies vapor-liquid-solid growth uses 3 phases: a solid crystal (or compound) of some material, a liquid catalyst, and a vapor precursor for the crystal. This thesis focuses on devices made from group IV semiconductor wires, namely silicon and germanium. To simplify the discussion silicon will be used as the example solid crystal. In most cases silicon and germanium growth

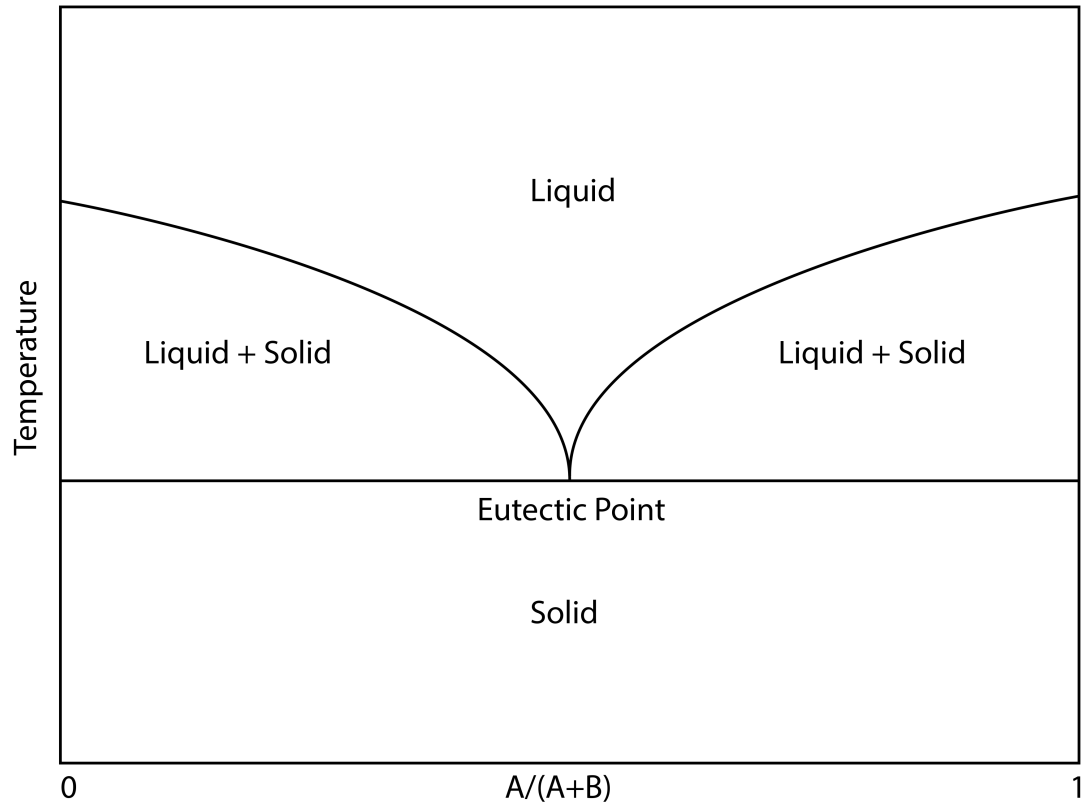

Figure 2.1: A simple phase diagram of a binary mixture that contains a eutectic point.

are similar though there are some important differences which will be noted during the discussion.

Before tackling the main topic of VLS it is instructive to consider simply the liquid-solid system of the metal catalyst and the solid crystal. Consider a system of any two materials in which there is a eutectic point (Figure 2.1). That is a point in which an alloy of the materials forms a liquid at a lower temperature than the two individual materials. Consider a small pure metal disc deposited on a clean pure crystal surface with the combined system at a temperature much less than this eutectic point. In this state the system is stable, laying a gold foil on a silicon wafer at room temperature does nothing to the silicon or the gold, the same is true in this thought experiment so far. However even at room tem-

perature there is a vapor pressure of each material and a diffusion rate, the reason nothing happens is that the exponential activation of these properties is so small that the probabilities are such that nothing measureable of consequence happens. This is not the case if in place of a solid we place a liquid on the crystal surface. The liquid's inherent molecular or atomic motion combined with bonding immediately manifests itself in terms of a contact angle. This angle between the liquid and solid on the atomic scale has to do with a competition in bonding between the contents of the liquid and the solid. If the liquid's contents can reduce their free energy by bonding with the solid surface they will wet the surface. If the liquid's free energy is lower by bonding with itself in the upper limit it will turn into a sphere. This is the competition between wetting and surface tension, which is important in VLS. It is important to note here that this change is entirely a surface or interfacial interaction that has ramifications over distances much greater than an atomic layer. Consider a more easily observable system where the limits of this behavior can be viewed: a clean silicon wafer. If dipped in hydrofluoric acid (HF), such a wafer will become hydrogen terminated. When water is placed on it the water has nothing to bond to and thus surface tension turns the water into a sphere. If instead the wafer has a thin layer of silicon oxide there will be dangling bonds for the water to bond with and the water will wet the surface. The interplay between the free energies of the different bonding configurations will determine the exact contact angle and wetting what is more important for VLS is the qualitative distinction between conditions in which wetting is favorable or unfavorable.

Returning to the small metal disc on the clean crystal surface we may realize that if we reach the eutectic point or near it similar properties will emerge. We may observe this behavior simply by heating the system. At low temperatures

the system is completely segregated with a pure metal disc and a pure crystal. As the temperature increases this will no longer be the case. Although the details will depend on the exact phase diagram in all cases there is a chemical potential which will drive diffusion as the system is heated. This will cause the metal to diffuse into the crystal and the crystal atoms to diffuse into the metal. What is more interesting than this bulk diffusion however is what happens at the surface. What happens here depends on exactly how the surface is terminated. Even if it is the same exact crystal the crystal orientation will make a difference as it impacts the density of surface bonds available to interact with the metal atoms. However in general qualitative terms the materials will either wish to wet or they will not. In the former case surface diffusion is important.

From the outlined discussion we can see that as we heat the metal disc on the clean crystal surface the materials will interdiffuse. As the eutectic point is approached in phase space the metal surface mobility will increase allowing surface tension to play a role in the shape of the metal particle. The exact shape will depend on the competition of wetting forces with surface tension. When enough interdiffusion has occurred the metal particle will melt. Because a liquid has an extremely high diffusion rate this melting will occur rapidly from the bottom surface liquefying the entire particle.

If the temperature is held exactly at the bulk eutectic point (and the particle is large) then the composition of the liquid and solid are known. The bulk eutectic point shown in bulk binary phase diagrams however neglects surface effects. As noted throughout the discussion so far surface effects are present. On the scale at which VLS is done today these surface effects are important. In the case of the Ge-Au system they effectively lower the eutectic point [14] from its bulk

value.

Another important size effect is simply that of material loss. Consider again the now melted metal particle on the surface. In the liquid phase the diffusion constants are very high. Meanwhile an isolated metal particle on a clean crystal surface sees a vast ocean of material. Given enough time at any temperature it will diffuse into a uniform background. At high temperatures with a highly mobile liquid this can occur quite rapidly.

So far we have considered only a single metal disc/particle on a clean surface. This limit is sometimes the case in VLS growths. Often times however it is not and there are neighboring particles. In this case the situation is slightly more complex. Consider a bulk crystal with two melted eutectic particles. Let the surface have some desired equilibrium surface coverage of the metal and let there be some diffusivity at the eutectic temperature. Further let the two particles be of different sizes. Surface tension can be viewed as a potential energy that drives the system to minimize its surface area. If we consider the two particles a single system then if they were touching they would merge and form one new larger particle with minimal surface area that satisfies the other boundary conditions of the system. If they are not touching they still interact but through the surface. The large particle will become larger at the expense of the small particle becoming smaller; this is Ostwald ripening [15]. This process is mediated in VLS primarily through the surface with both particles constantly loosing material to the surface and each other, the larger surface area of the large particle simply allows it to loose less per volume and thus grow relative to the small particle.

To make the above discussion more concrete consider the Au-Si system (Fig-

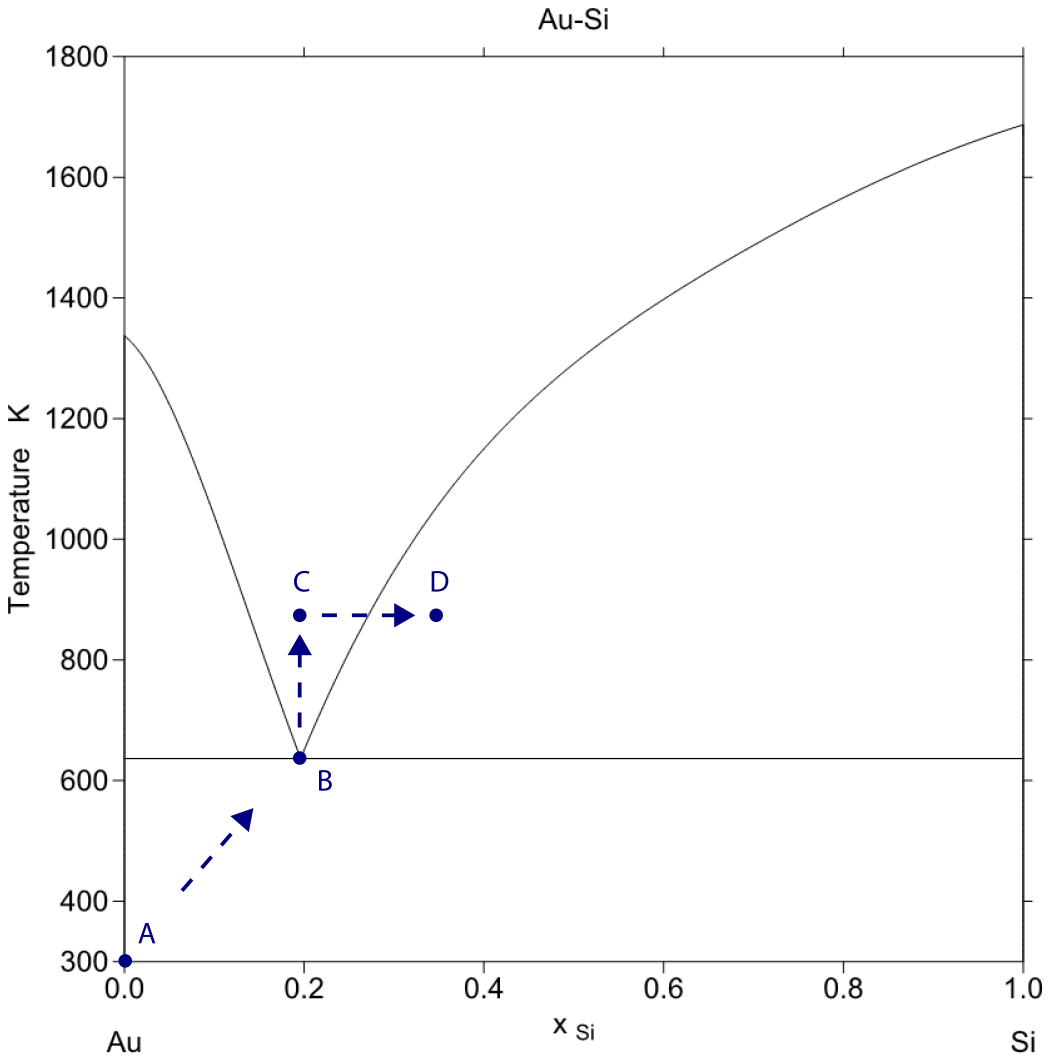

Figure 2.2: Phase diagram of Au-Si adapted from [16]. For a VLS growth the two materials (Au catalyst particle and Si wafer) start at point A completely phase separated and solid. As the materials are heated diffusion increases the concentration of Si in the Au, once the eutectic temperature is reached the the Au particle rapidly will melt moving to point B (the eutectic point). If the temperature is increased further the mixture will be somewhere in the liquid phase represented by point C. Once SiH_4 or another precursor is turned on the concentration of Si increases in the particle eventually reaching a point to the right (shown as point D) of the phase boundary resulting in a solid crystal being precipitated from the catalyst.

ure 2.2), perhaps the most common of all VLS systems studied. Further consider an array of identical particles of pure Au placed on a clean silicon surface in a perfect vacuum. Au wets clean silicon. The exact surface coverage depends on the exposed crystal surface and termination [17]. If heated the silicon from the wafer will diffuse into the Au (and the Au into the Si) until the Au melts. As this occurs the Au will start to migrate onto the surface to satisfy this surface coverage. Particles in the middle of the array will quickly coat the surface in between the particles. Because all of the neighbors are identical they will not lose any Au to their neighbors. Thus they will only loose Au to the bulk Si wafer. However particles near the edge of the array are different. They do not have nearest neighbors; they have an expanse of Si which needs the aforementioned surface coverage to be in equilibrium. This surface diffusion shrinks the particles and they eventually disappear completely under simple annealing if the time is long enough. This effect propagates inward from the outside of the array. Taken in aggregate the outer particles can be seen as screening the inner ones with the effect attenuated over some screening length. We will see this surface physics both in arrays of many particles as well as the single particle case in the growth experiments later in this chapter.

Up to this point we have only discussed the liquid-solid part of the VLS system. Now we turn our attention to the vapor phase. Typical VLS has a lot in common with low pressure chemical vapor deposition (LPCVD). It could in fact be called catalyzed CVD, as it behaves very much like a much higher temperature CVD process localized at the catalyst. Therefore it is instructive to consider regular CVD first. In regular CVD there is a vapor precursor to the deposited material. A wafer is placed in the CVD reactor and this vapor precursor has some affinity for the wafer's surface. The vapor precursor interacts with the

surface and may wish to bond with that surface. To do this the precursor must break bonds within the precursor before bonding with the surface. This process is facilitated by thermal (LPCVD) or other energy (e.g. plasma enhanced CVD). The growth rate of CVD depends on the probability of breaking the precursor bonds and forming new ones with the surface. The probability of breaking bonds is increased by increasing the temperature, while the probability of forming new bonds is greatly affected by the hybridized bonds that occur when the molecule and wafer surface are in intimate contact. Again here surface physics is very important. A monolayer surface coverage can greatly change the rate of CVD and other vapor phase deposition methods. Good examples are graphene where atomic layer deposition (ALD) is ineffective as there is nothing to bond to [18], and the growth of heavily *n*-type Si with P as the dopant where the P frustrates Si growth in LPCVD.

Common VLS can be viewed partially as a modification of this surface interaction. Consider the case of the SiH_4-Au-Si system. The silane sees a gold surface rather than a Si surface where VLS is occurring. The affinity of this surface to break a precursor's bonds depends on the details of the valance interactions and is a topic onto itself. What is important is that useful catalysts for VLS break the precursor bonds more readily than the bulk precipitated crystal surface. In most cases in VLS both bulk growth and VLS catalyzed growth occur simultaneously. The ratio of the growth rates depends on the reactor conditions. These conditions typically are the reactant partial pressures, the total pressure, and the temperature.

When VLS is occurring the vapor precursor bonds or cracks at the surface of the catalytic particle. If there were no other effects then this would lead to

a higher concentration of the precursor at the surface of the eutectic particle. In reality diffusion in the liquid phase rapidly makes the concentration in the particle nearly uniform. Consider again the SiH_4-Au-Si system and the phase diagram shown in Figure 2.2. As Si is absorbed into the Au from the saline vapor the concentration in the particle goes up. Referring to Figure 2.2 if the precursor is turned on at point C then the presence of the precursor drives the particle toward point D. As the particle's Si concentration crosses the equilibrium phase transition line Si will begin to precipitate out of the catalyst. This material will precipitate out onto the surface that minimizes its free energy. For a confined particle this free energy has contributions from both the edge facets of the crystal and the surface [19]. As VLS continues this process results in a dynamic equilibrium to the right of the equilibrium phase transition line that results in a rapidly growing extruded crystal.

This process has some additional interesting properties to note. The rate of VLS like its bulk CVD cousin depends on temperature with increasing temperature increasing the growth rate. However VLS has a nucleation time associated with it. This is the time required to change the concentration of the catalyst from point C in Figure 2.2 to point D. Because the absorption of material occurs only at the surface of the catalyst this time is longer for larger particles because of their greater surface to volume ratio. However, once the point where a crystal begins to precipitate out is reached particles regardless of size grow at approximately the same rate. This is because the particles are nearly the same shape and the ratio of the precipitating surface and the absorbing surface is nearly a constant (if the shape were exactly fixed it would be a constant). This holds for crystals growing in the same orientation but of different diameters. As the particle size changes different growth directions become energetically

favorable [19]. This changes the growth rate as the interplane spacing and bond density and thus free energies are different. A secondary effect which changes the growth rate as the orientation changes is that the side facets of the precipitated crystal are different which changes the shape of the catalytic particle, and thus the surface area ratio. However in all cases a hemispherical particle is a good approximation.

As the crystal grows the surface diffusion of the catalyst can continue via the sidewalls of the wire. This effect depends on the reactor conditions which modify the surface termination and the crystal facets which are present.

2.3 Vapor-liquid-solid growth in practice

The preceding discussion has covered the major physical considerations needed to understand VLS growth in the context of this work leaving us free to consider actual implementation of this process in practice. With 48 years of publications available on the topic one might expect that implementation of VLS is straight forward. It certainly can be, however before discussing results of particular implementation it is worth noting the systematic considerations of a CVD reactor.

As noted VLS depends on essentially 3 parameters after the precursor, catalyst and substrate are chosen, the temperature of the substrate, the pressure in the reactor and the partial pressures of the reactants.

In practice VLS is typically carried out in a linear tube furnace reactor such as the ones illustrated in Figures 2.6 and 2.10. The reactor has an inlet for the gases at one end and a pump at the other. In between these ends it is heated by some

means, commonly joule heating, resulting in the walls of the quartz obtaining a high temperature. The reactive gases are injected into the tube at the intake end and flow viscously (in the pressure regime used most commonly) to the outlet/pump end. These gases are typically injected at a fixed rate measured with reference to hydrogen in so called standard cubic centimeter per minute (SCCM).

In such a reactor it is worth considering how well the 3 parameters are known. Starting first with the pressure, we can see immediately that if we are flowing the gas in the regime where pumping occurs by viscosity there will be some pressure gradient driving this pumping. This effect while present and unavoidable is not significant in a well-designed reactor in steady state.

Next consider how well the temperature of the substrate is known. Typically in these systems the temperature of the reactor is measured by thermocouples both inside and outside the tube. There are several means of exchanging heat in such a system; under the highest vacuum levels the principle exchange means is radiative; at higher pressures the conductivity of the gas becomes important. In the radiative case the emissivity of the structures being grown is relevant as is the contrasting emissivity of the catalyst and substrate. These issues complicate knowing the exact temperature of the reaction area; however in tube thermocouples do typically give a close estimate of the actual temperature. The larger issue in reproducing the results found in the literature is the large systematic offsets in temperature that are encountered due to placement of the thermocouples. In many cases small systems built for research lack in tube thermocouples and instead the temperature outside the tube is reported. This is generally higher than the actual temperature of the reaction. Because the reactions and

diffusion processes are exponentially activated this is a significant issue, even a few degrees can greatly change the results of a VLS growth as we will see.

Finally there is the partial pressure. The partial pressure of a reactant may intentionally not be the full pressure of the reactor chamber for a variety of reasons including safety. Such intentional dilution is known before hand; however in a reactor the reactants can also be depleted. In a linear reactor the mixture and exact partial pressure is only known at the inlet, as the reactants flow through the system they will decompose and thus the partial pressure is a function of displacement in the tube. Only in the case were a perturbative amount of the reactant is used is it truly correct to assume the partial pressure is known precisely. This is a significant issue, although it is typically gauged by the uniformity of the background CVD growth, the background CVD rate is also a strong function of temperature which itself is non-uniform in a typical reactor. One means to alleviate this issue would be to sample the composition of the gases at the outlet however this is almost never done in practice. This issue is worthy of note because many reactors are operated in such a manner as to flow the minimum SCCM of precursor gases. This is a cost saving measure but it hampers the reproducibility of results across reactors. The partial pressure of the precursors strongly affects the nucleation time and growth rates of VLS. The result of these systematic considerations is simply that published reactor parameters can be viewed more as a guide to where in parameter space a result might be achieved rather than an exact recipe for a result.

To produce semiconductor materials via VLS catalysts are needed. These catalysts can be a wide range of metals; in this work only two are used: Au and Al. Catalysts can be placed on a substrate by a number of means, the most

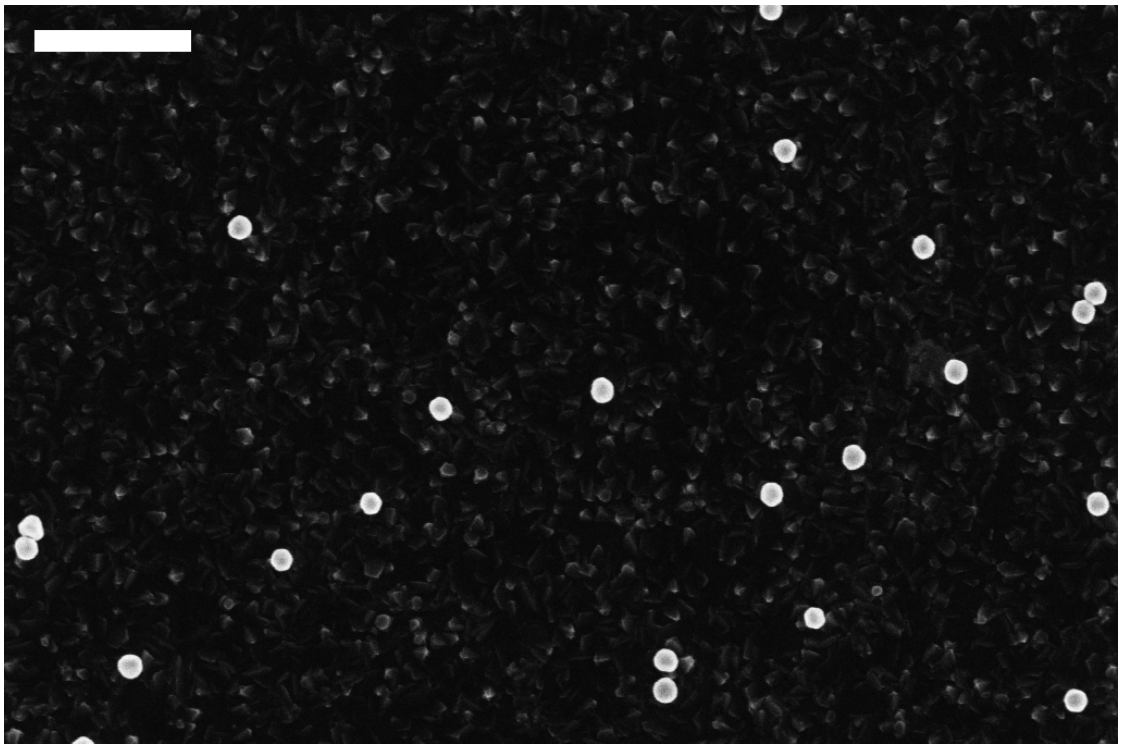

Figure 2.3: 100 nm colloidal Au on a Ti thin film showing both isolated and aggregated particles. The scale bar is 800 nm.

common of which are the deposition of colloidal particles, thin film deposition and lithographic patterning.

Colloidal particle sources for catalysts are convenient in that they allow for well-defined diameters of particles to easily be dispersed onto a substrate. Such particles are commercially available in monodispersed solutions. To deposit particles onto a substrate the solution is simply placed in contact with the substrate for a desired time. Several methods are used to enhance the number of particles that adhere to the substrate which will be covered in the experimental sections that follow. Colloidal particle depositions (Figure 2.3) typically exhibit a low density of particles, when particles are near one another they tend to aggregate into clusters. Another property of note for colloidal sourced growths is the presence of carbon in the form of organic ligands on the colloids.

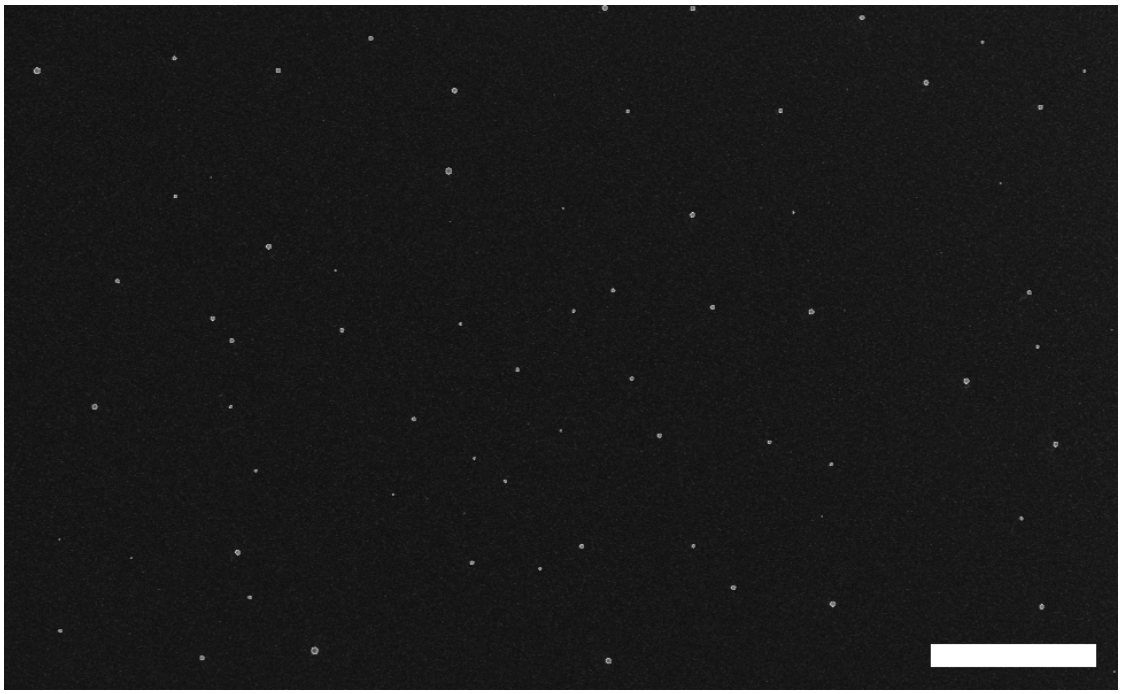

Figure 2.4: A 10 nm thick evaporated Au thin film on Si has been annealed to break the film into islands. The islands form with a distribution of diameters with larger particles ripening. Long anneal times and/or high temperatures result in larger particles and greater inter-particle spacing. The scale bar is 8 μm.

Blanket thin films of metals are another source of catalyst for VLS growth. For very thin evaporated films islands naturally form which create isolated catalyst sites for growing VLS wires. For thicker thin films annealing can be used to break up a thin film and aggregate larger islands (Figure 2.4). This works particularly well when the substrate is composed of a material that will form a eutectic with the metal, as the liquid has significantly greater surface mobility.

Finally catalyst can be deposited in a pattern via lithographically defined means. This could be a lithographically made shadow mask, a liftoff process (Figure 2.5) or a negative lithographic process involving etching. Each is capable of producing the isolated catalyst sites needed to create VLS materials.

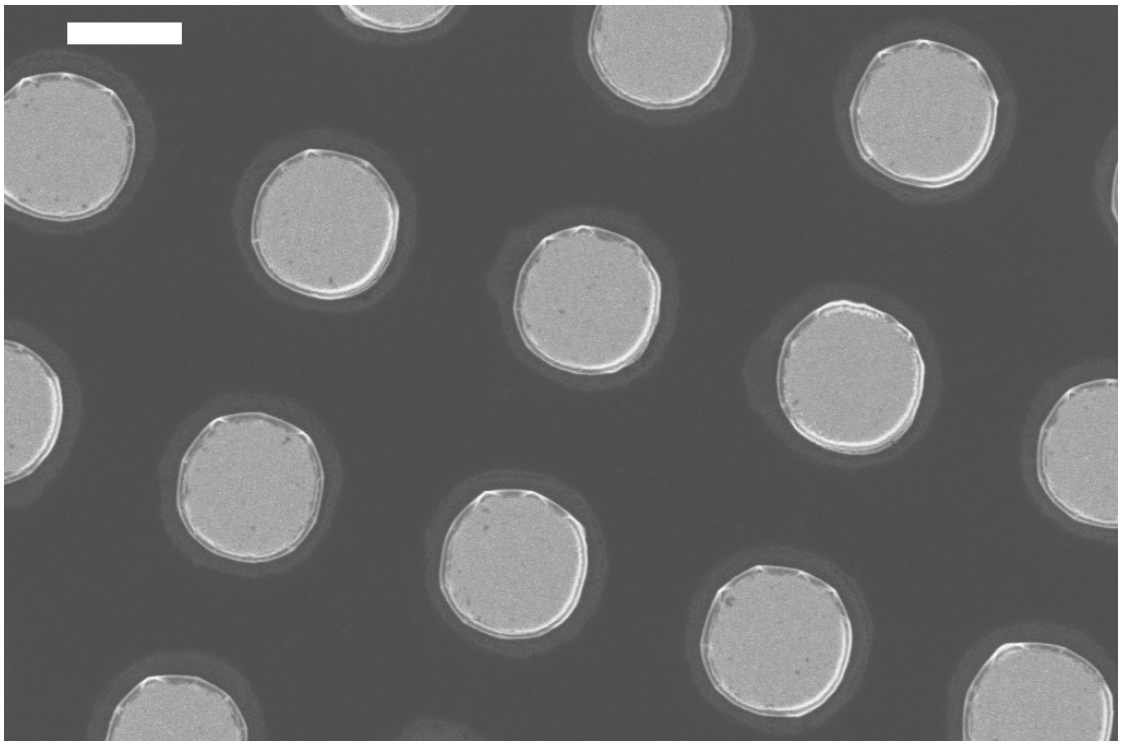

Figure 2.5: Lithographically defined catalyst sites created using an oxide based liftoff process. For this process HF provides an undercut seen as the non-uniform ring around each Au disk. When annealed these thin disks must first form hemispheres before growing VLS wires otherwise more than one wire will be grown. The scale bar is 1 μm.

2.4 Park group reactor

Having covered the general means of creating catalyst patterns and the general systematic issues with CVD reactors applied to VLS it is now possible to cover actual experiments. For all of the experiments reported in this thesis two reactors were used the first of which was constructed by Prof. Park's group at Cornell.

This reactor (Figure 2.6) consisted of a simple array of mass flow controllers, a 1 inch quartz tube furnace and roughing pump connected to a throttle valve for pressure regulation. The system was loaded manually each time with the

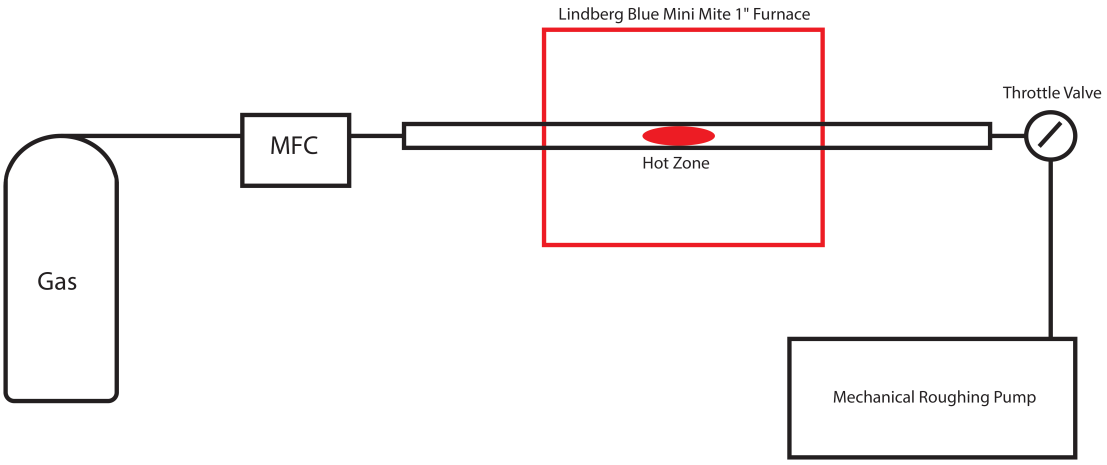

Figure 2.6: A schematic representation of the LPCVD nanowire reactor in the Park group lab at Cornell. The reactor has a set of process source gases represented by a single gas bottle here connected to a stainless line via a mass flow controller. This mixed gas line enters the reactor which is a 1″ diameter quartz tube and flows through the hot zone where the sample sits. It is pumped at the other end of the tube via a mechanical roughing pump which is regulated via a throttle valve. The hot zone is fairly small in this reactor making it sensitive to sample placement. In this reactor the entire tube is removed to load each sample and must be cooled down and warmed up for each synthesis. The seals are simple viton gaskets at each end of the quartz tube.

seals to the tube broken for each sample loaded. The furnace used to heat the tube was a 1″ Lindberg Blue Mini Mite. This setup suffered from many problems related to the small volume and design. Growth substrates were limited to less than 1″ in diameter and could not be particularly long either given the small hot volume of this furnace. The tool lacked any means of holding a substrate in place often resulting in samples shifting due to pressure pulses in the tube. In addition this reactor was never capable of growing Si VLS materials. Bulk CVD growths of Si were also poor. Retrospectively I conjecture this was likely due to oxygen leaking into the system. The system was able to grow quality Ge nanowires and was used in this capacity. The ability to grow Ge nanowires is consistent with the suspected oxygen level as germanium's affinity for oxygen is much lower than silicon's.

Initial work in this reactor was performed using colloidal Au particles on <111> Si wafers using 1.5% GeH_4 in H_2 as the precursor. To enhance the density of colloidal particles precipitating from the solution both acidification of the solution by adding hydrofluoric acid (< 20:1) and the addition of poly-L-lysine (0.1% w/v) were used. Particles from 20-200 nm were used in different experiments but primarily 40 and 80 nm particles were used as parameters were found early on that allowed the growth of Ge wires from these particle sizes. These parameters were provided by Mark Levendorf who was the principle operator of this CVD tool in the Park group. The typical window for growth of this type of wire was found to be 290-350 C with a total pressure in the 100-200 Torr range. Considering the dilution this pressure corresponds to a partial pressure of 1.5-3 Torr of GeH_4. A typical example of this type of growth can be seen in Figure 2.7. From the SEM images we can see the aforementioned low density of wires formed by this method. Also notable are the fine wires and the variety of orientations observed.

For any wire diameter there is a growth direction that will minimize the free energy of both the flat growth interface and the side facets as noted in the theory portion of this chapter. For some diameters however there are multiple orientations with similar free energies. Registry of any orientation to the substrate requires intimate contact between the catalyst and the wafer. The use of poly-L-lysine and the carbonaceous ligands of the colloid both contaminate the surface of the wafer and interfere with this intimate contact. To reduce the impact of this issue hydrogen was used to anneal samples prior to growth at elevated temperatures (< 400 C). This reducing atmosphere in principle removes the majority of the carbon. However many forms of carbon are not reduced in these conditions, and such residual carbon is the most likely cause of both the Au fragmentation

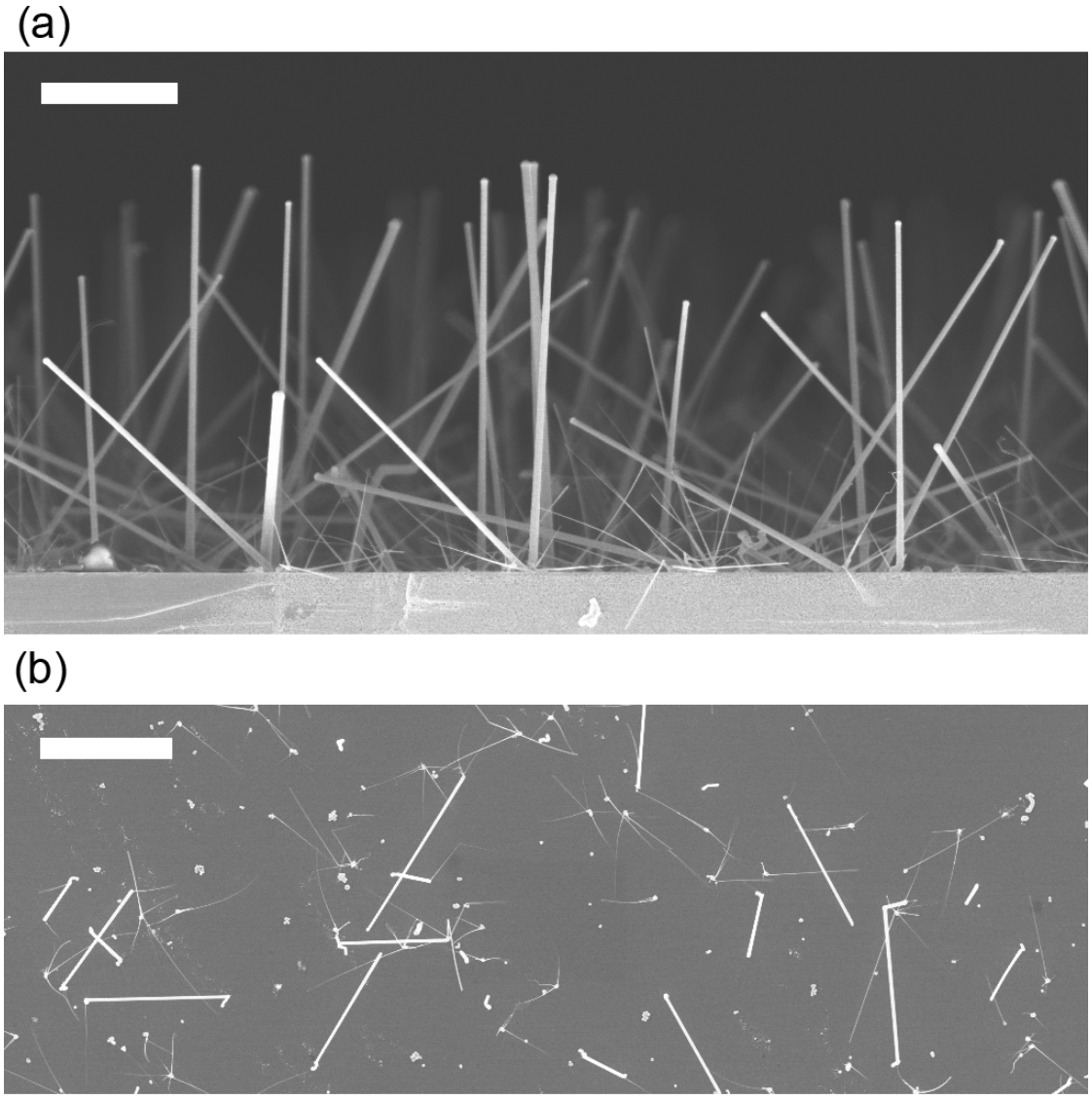

Figure 2.7: Plan and side views of a typical Ge nanowire growth from colloidal Au in the Park reactor. The wires are of high quality as seen in the side view (a). The apparent high density of the side view is deceptive, and caused by the deep depth of focus of the SEM. A plan view (b) shows that the wire density in this growth is actually quite low. Dots in this view are the vertical or near vertical wires. The scale bars are 2 and 4 μm for the side and plan views respectively.

which is the source of the small wires observed and the wide variety of growth directions that are unregistered to the substrate.

One of the main aims of my research was the creation of materials for photovoltaic applications. In this area cost is paramount and the use of a single crystal substrate makes little sense if the device is to be mass produced. This is because the material quality of a single crystal substrate is typically significantly better than that of the VLS wires themselves suggesting it would be better to use the substrate itself for the photovoltaic rather than the VLS wires. However it should be noted that work has been done to reuse such a substrate wafer mitigating the cost overhead of this approach [20]. Because of this consideration low cost substrates such as metals and glass are attractive.

With the Park group reactor the growth of Au catalyzed Ge wires on metal surfaces was explored. In general this system is ternary in nature with an alloy of the two metals in question forming in parallel with the eutectic. Because of this complication this type of growth is generally problematic. The exceptions to this appear to be metals with a stable oxide that cannot be reduced at the temperatures used for VLS. A typical result for a system where the alloying of the metals occurred can be seen in Figure 2.8. Although we clearly see extruded structures that indicate a VLS related process has occurred they do not appear to be crystalline as they are neither straight nor faceted. This result can be contrasted with the use of Ti as the substrate material. As can be seen in Figure 2.9, growth of Ge wires on Ti results in many straight faceted crystals. I decided to study this system further via the use of transmission electron microscopy (TEM). The results of this study are contained in chapter 3.

Although the metal film results particularly the Ti-Au-Ge system were inter-

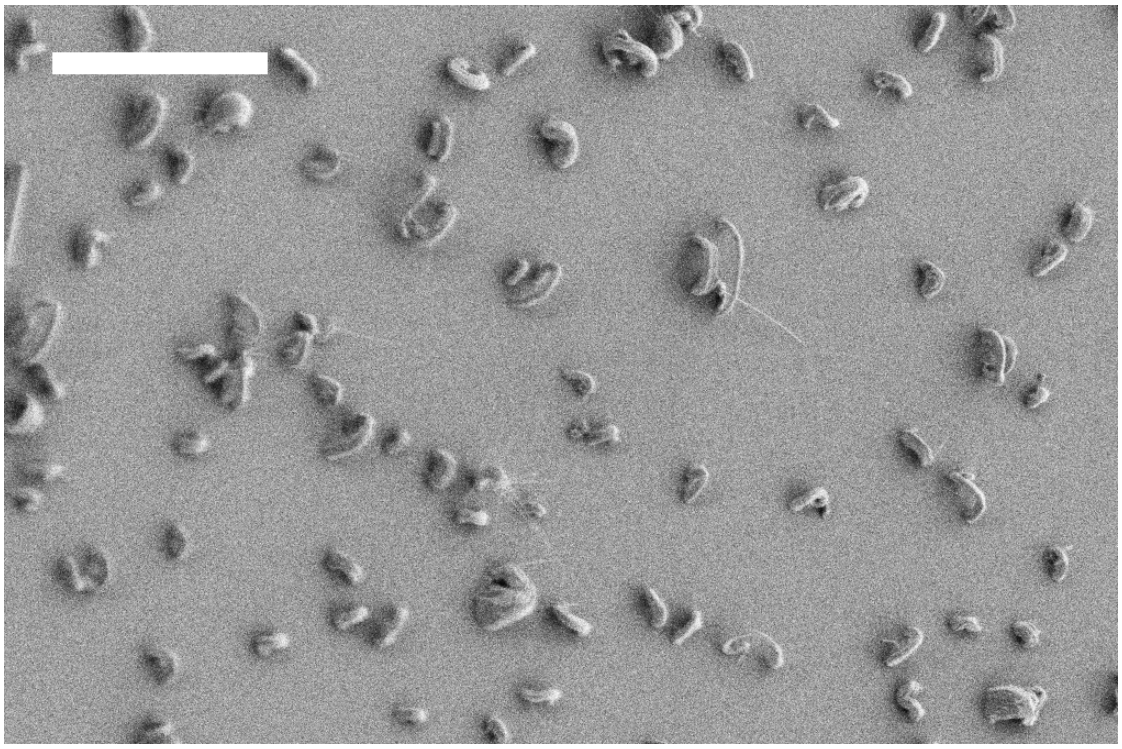

Figure 2.8: This SEM shows the result of an experimental VLS growth using Mo as the substrate. The catalyst was colloidal Au and the precursor was dilute germane. As can be seen the resulting growths lack facets which would indicate crystal material and therefore are likely germanide. The scale bar is 4 μm.

esting the Park group reactor was not adequate to make significant progress on the creation of effective photovoltaics, both due to its limited growth volume and the fact that it was unable to produce quality Si films. This led to the start of an additional collaboration with IBM Research at Yorktown Heights.

2.5 IBM Yorktown Heights reactor

The reactor at IBM Yorktown Heights (Figure 2.10) is vastly different than the academic Park group reactor. It was designed to semiconductor specifications to be relocatable into a manufacturing facility, and is able to grow materials on

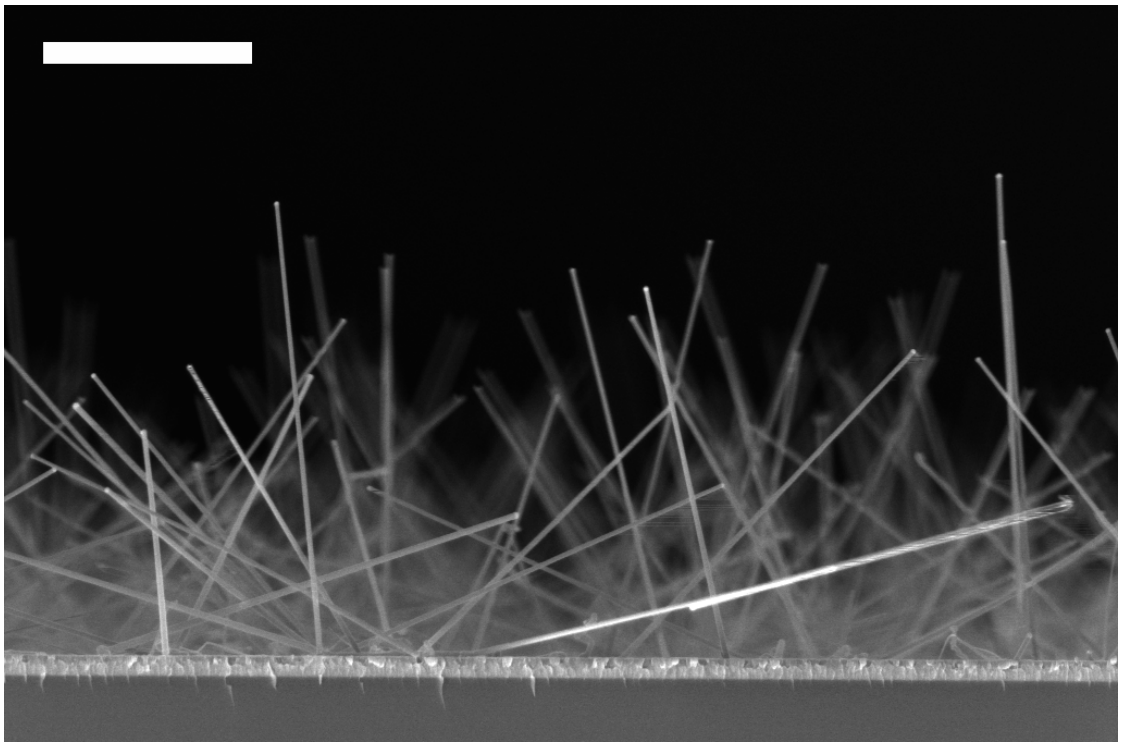

Figure 2.9: It is possible to grow long faceted Ge nanowires on Ti thin films as seen in this SEM. The scale bar is 2 μm.

200 mm wafers. The tool is a UHV based system with a UHV load lock. This load lock contains a thermal evaporator allowing for catalyst deposition without breaking vacuum. This is essential for the the growth of Al catalyzed wires [21]. Other materials can of course be evaporated as well. In the context of this work Au was also deposited in some cases using the load lock evaporator.

It is worth considering the advantages and disadvantages of UHV to VLS at this point. In the case of Al catalyzed wires it is essential to prevent the oxidation of the Al which in turn would prevent VLS. However for Au catalyzed wire UHV is not needed. In a very clean system Au is free to diffuse across the surface of a wafer as discussed in the theory section of this chapter. This effect continues as the wire grows via the wire sidewalls [22]. This can be a negative effect in many practical cases. However the migration of Au on the

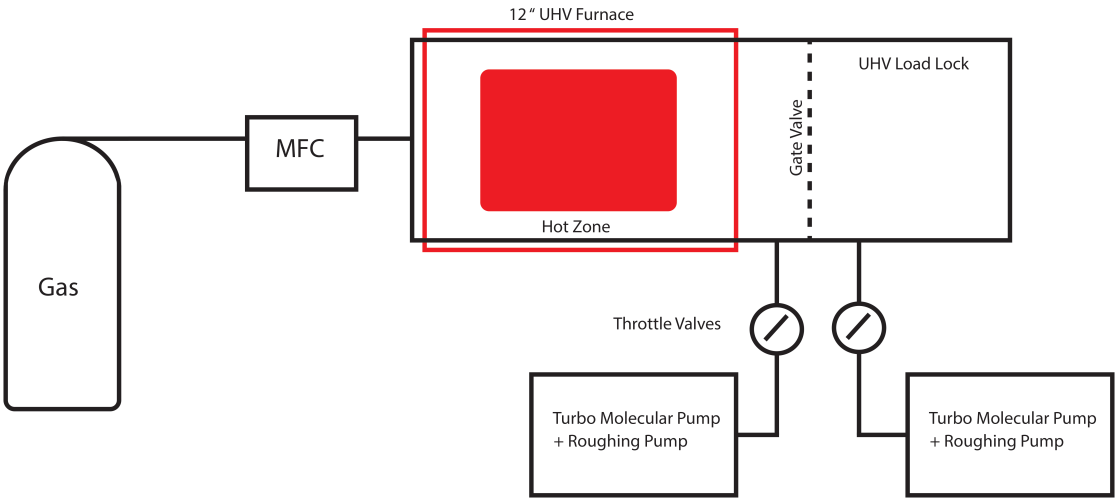

Figure 2.10: A schematic representation of the UHV-CVD nanowire reactor at IBM Yorktown Heights. The reactor has a set of process source gases represented by a single gas bottle here connected to a stainless line via a mass flow controller. This mixed gas line enters a large 12″ quartz tube furnace with water cooled seals. The tube is kept under UHV pressures via a turbo-molecular pump backed by a mechanical roughing pump. The system is able to remain at elevated temperatures and low pressures via the use of a UHV load lock. The system supports 200 mm wafers and contains a thermal evaporator in the UHV load lock. The hot zone is larger than the wafer and positioning is reproducible via quartz load arm with fixed pins for positioning the 200 mm wafer. Samples smaller than 200 mm are placed on a carrier wafer.

surface is strongly affected by the termination of the surface and in turn the reactive atmosphere [17]. A reactor with a higher base pressure of oxygen or other contaminates can prevent Au migration by modifying the surface termination during synthesis. This is a potential advantage of having a higher base pressure in a reactor, however as can be seen from the Park group reactor too many contaminates can make VLS growth impossible in the case of Si.

These considerations are largely theoretical as the actual reactor has no facility to controllably manipulate such contamination. As a result Au migration and surface diffusion are major effects in this reactor.

The remainder of this chapter consists of sections considering VLS experi-

ments to grow particular types of materials in this reactor. All of the material used in publications during my thesis except for the initial TEM study in chapter 3 which was grown in the Park group reactor was produced using the Yorktown reactor. The reasons behind each type of VLS growth will become clear in the subsequent chapters of this thesis. They are presented here with limited context in an attempt to contain the discussion of VLS growth experiments to a single chapter rather than as an extended discussion in each chapter.

2.6 Silicon vapor-liquid-solid growth on metal thin films

When I first began work with Mark Reuter and Brent Wacaser at IBM on VLS wires I had just completed the TEM work that is the subject of chapter 3. As a result I was keenly interested if this result could be extended to work with Si. Although it was possible to reproduce the Ti-Au-Ge result at Yorktown, initial work with Si was not successful. Ni, Mo and Ti thin film substrates were tried in combination with Au colloids without success (Figure 2.11). These metals were chosen for study because of their well-known silicides which would enable reasonable contacts for final devices. The reason for the failure of Ti-Au-Si is likely the higher reaction temperature for the VLS growth. While Ge can be grown with GeH_4 at nominally 300 C, Si grown with SiH_4 requires temperatures in excess of 425 C. Buffer layers of a-Si were added on top of the metals in an attempt to mediate ternary alloy effects but also were unsuccessful. As work in other areas was proving more fruitful this line of study was abandoned.

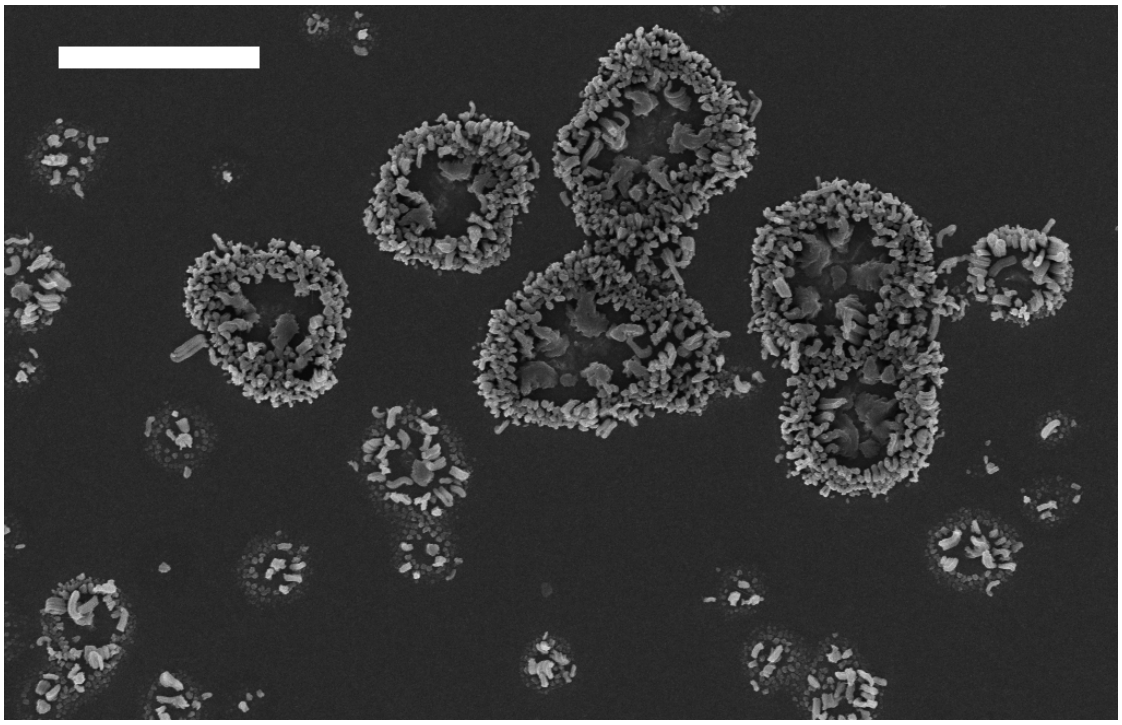

Figure 2.11: Although the Ti-Au-Ge system is able to grow long faceted nanowires, the Ti-Au-Si system is not as seen in this micrograph. At the minimum temperature to break down saline thermally the Ti and Au appear to interact strongly. The scale bar is 4 μm.

2.7 Micron scale gold catalyzed silicon vapor-liquid-solid wires in large arrays

In parallel with the metal substrate work, growth experiments were begun to create Si VLS wires of large diameter. Parameters for growing VLS nanowires up to 100-200 nm were well known in the IBM reactor when I arrived. These wires were created by annealing nominally 2-3 nm thick Au thin films. By changing the annealing time and temperature different size islands could be formed to control the grown wire diameter with moderate spread (Figure 2.12). The trade-off in this approach given the fixed Au volume available is larger wires automatically mean lower density, which is a negative effect from the per-

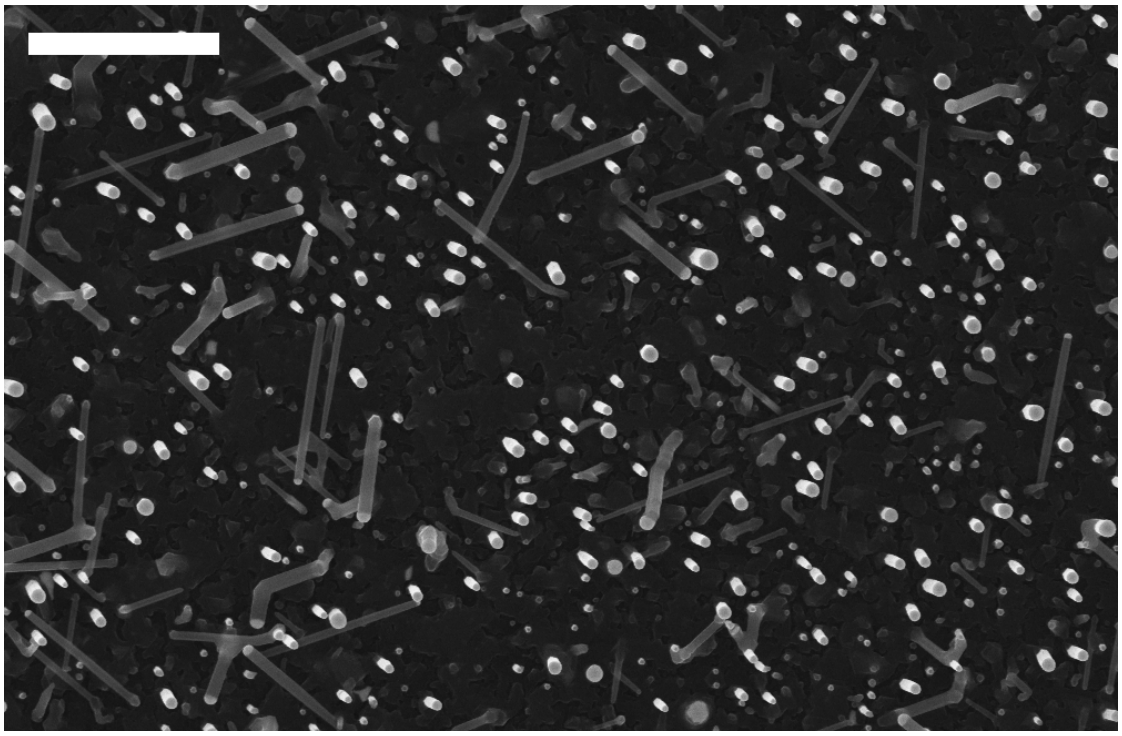

Figure 2.12: Seen here are Si nanowires grown from a thin film of Au which was annealed to break the film into islands. As seen in Figure 2.4 these islands result in hemispheres of different diameter and so the resulting VLS wires are also of different diameters with similar spread. The majority of the wire are growing vertically in the <111> direction. The scale bar is 2 μm.

spective of photovoltaic applications. As will be discussed in more detail in chapter 4, it is advantageous to minimize the surface area of a photovoltaic. It therefore follows that wires of larger diameter are desirable.

To this end I explored the CVD parameter space to grow larger Si VLS wires. To solve the density problem the catalysts used for these growths were defined lithographically. Work in the literature at the time [23] suggested that in such a system a SiO_2 buffer layer between catalyst sites was needed. Because of this requirement a liftoff process was developed which used SiO_2 as the undercut for the liftoff. This method provided not only the isolation layer suggested by the literature but also an extremely clean surface onto which the catalyst could

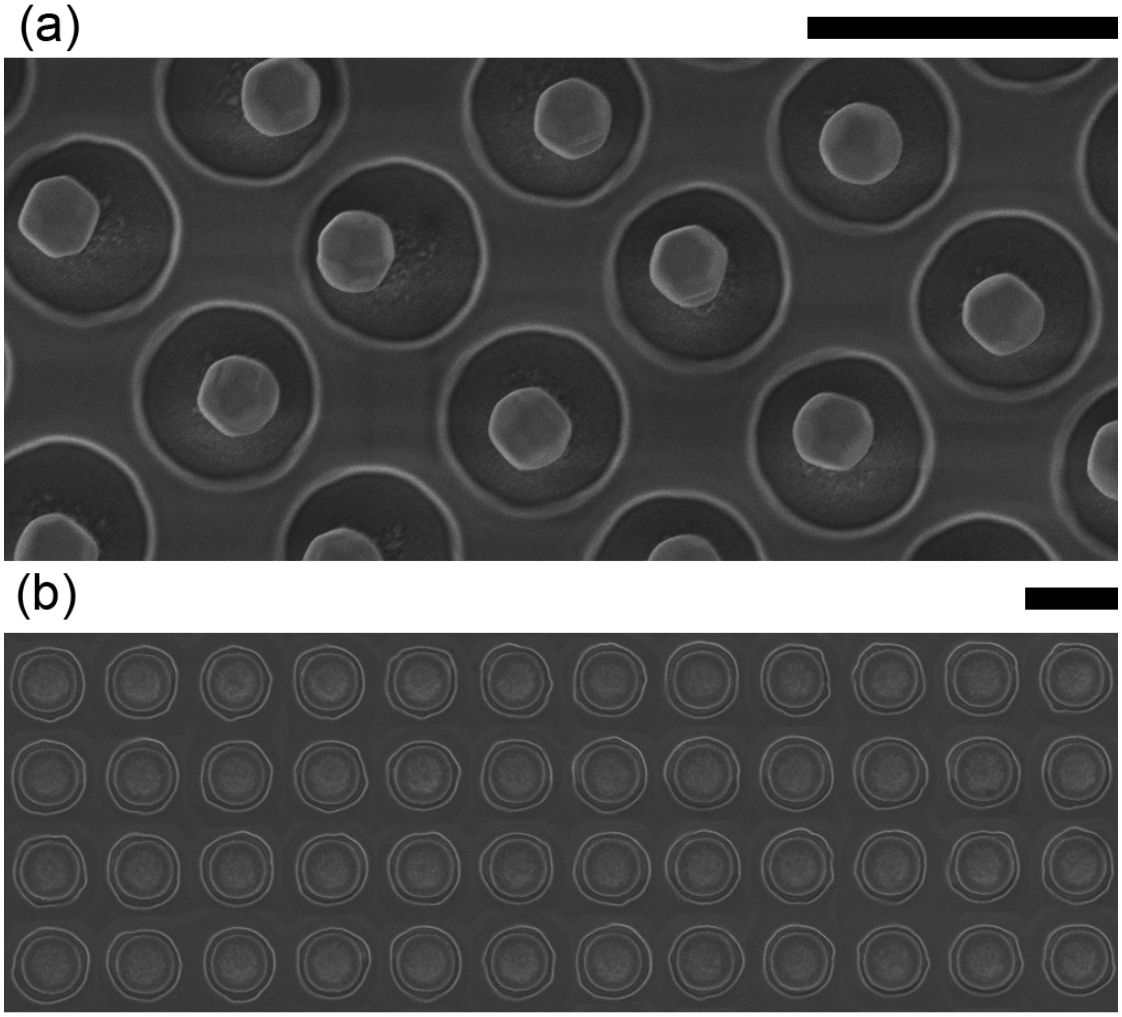

Figure 2.13: Au wets Si but it does not wet SiO_2. In (a) we see the result of an N_2 anneal test of Au performed in an SiO_2 well that was not completely clearer to the Si. This results in faceted spherical particles. In (b) we see the result of the same anneal/process when the wells are cleared to the Si surface. The scale bar are both 2 μm.

be deposited.

The process was used universally after it was developed. It consists of first completing an RCA clean on the substrate Si wafer. The wafer is then thermally oxidized to a thickness greater than the catalyst deposition will be. Resist is used to coat the wafer and patterned with a series of wells. These wells are transferred into the oxide layer partially using a CF_4 RIE. CF_4 should be used in

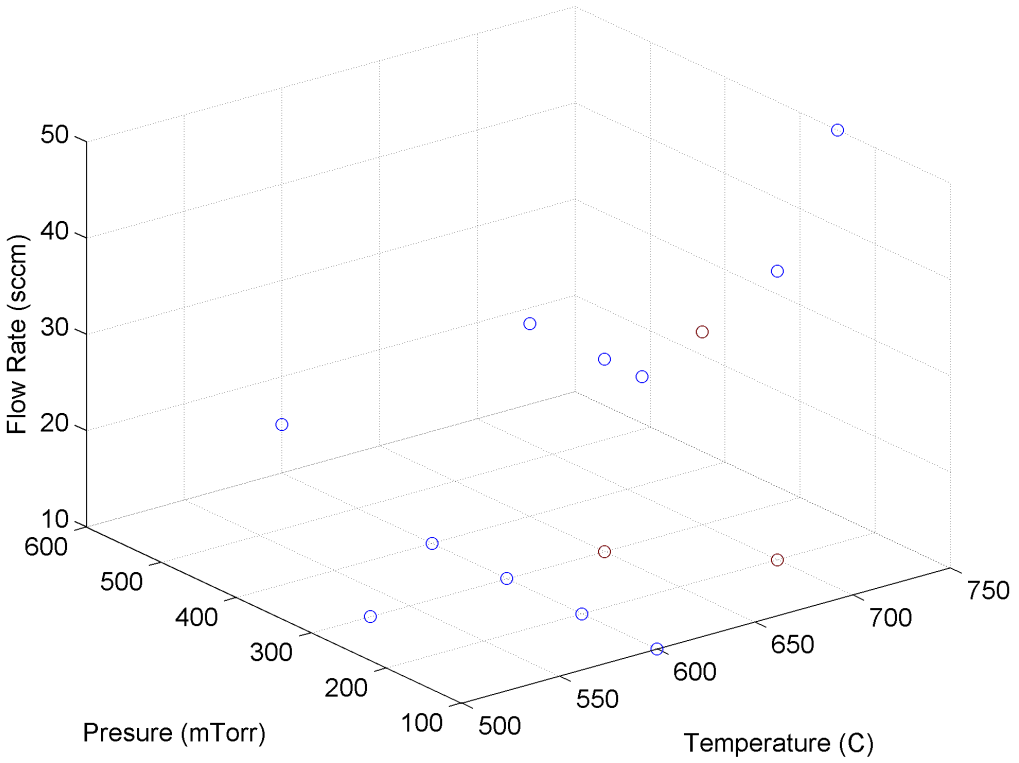

Figure 2.14: This plot illustrates the initial exploration of the VLS parameter space for the growth of microscale Si wires in the IBM Yorktown Heights reactor. The three main controllable parameters are pressure, temperature, and gas flow rate. In all cases undiluted SiH_4 was used and at the inlet represents the total pressure of the reactor. The points in red indicate growths were the SiH_4 was depleted in the growth and the partial and total pressures are no longer close.

place of CHF_3/O_2 to minimize any possible polymer deposition. Following the RIE step the wafer is dipped in HF. This step undercuts the resist layer, stops with high selectivity on the Si surface and hydrogen terminates that surface. Evaporation of Au always was done immediately after the HF dip with the wafer exposed to atmospheric oxygen for no more than 5 minutes. Annealing experiments reveal clearly when the Au is in good contact with the Si and when a residual oxide layer is present (Figure 2.13).

With this method of creating Au patterns an extensive search was made of

the VLS parameter space (Figure 2.14) for both annealing and reaction conditions to grow the largest possible wires. In general I found that larger epitaxial wires require higher temperatures for the catalyst/wire interface to remain stable. If the temperature is too low the catalyst site will fragment (Figure 2.15) or the wire will contain kink formations (Figure 2.16) from the instability of the catalyst/wire interface. Higher reaction temperatures require significantly higher gas flow to avoid depletion of the precursor (Figure 2.17). This was problematic due to the limited amount of SiH_4 allowed per bottle in this tool (a safety restriction). Annealing the catalyst at higher temperatures prior to growth also favorably reduces kinking as does the complete removal of the buffer oxide layer prior to growth. This last observation superficially contradicts results of the Atwater group. However it should be noted that Atwater's work uses significantly higher temperatures in conjunction with $SiCl_4$. This reaction system is significantly different from a SiH_4 based reactor with its lower temperatures. In the case of $SiCl_4$ the CVD growth of Si in the background during VLS can be manipulated due to the presence of reactive Cl which etches the Si in parallel to the growth. This can leave an oxide layer free of a Si thin film throughout a reaction. In a SiH_4 reactor this is not possible. Once the oxide layer is coated in a CVD film (which takes less than 1 minute with typical parameters) its utility as a buffer is limited. Thus it is often better to simply remove this layer completely before growth. An exception to this is when a very high temperature annealing step is desired before growth, in which case the oxide layer prevents Au migration and loss to the surface around the lithographic site. In these cases the oxide layer should be made as thin as possible to reduce the probability of the catalyst touching and sticking to the sidewall surface of the oxide well which can create kinking defects.

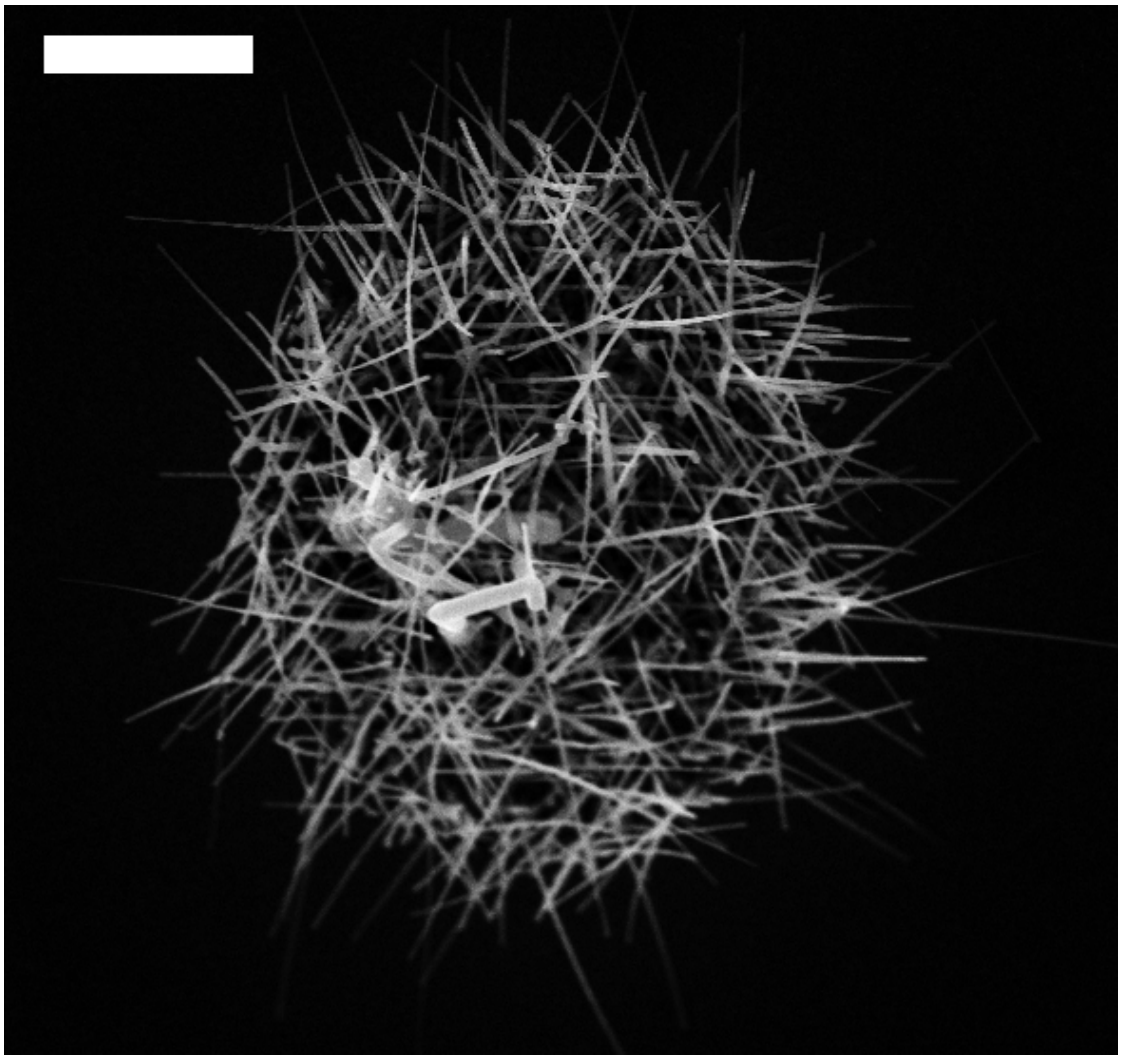

Figure 2.15: When the temperature of the reactor is set below that needed to uniformly mix the eutectic or to form a single droplet, many small wires will grow as seen in this micrograph. The scale bar is 4 μm.

Notable in the experimental results is the consistent contrast ring observed in SEM around the wire arrays and the small diameter or absence of wires at the edge of arrays (Figure 2.18). These effects are due to Au loss to the surrounding clean Si surface. As discussed in the theory section of this chapter this surface is a significant sink of Au.

Excellent results are achievable with optimization of the growth parameters.

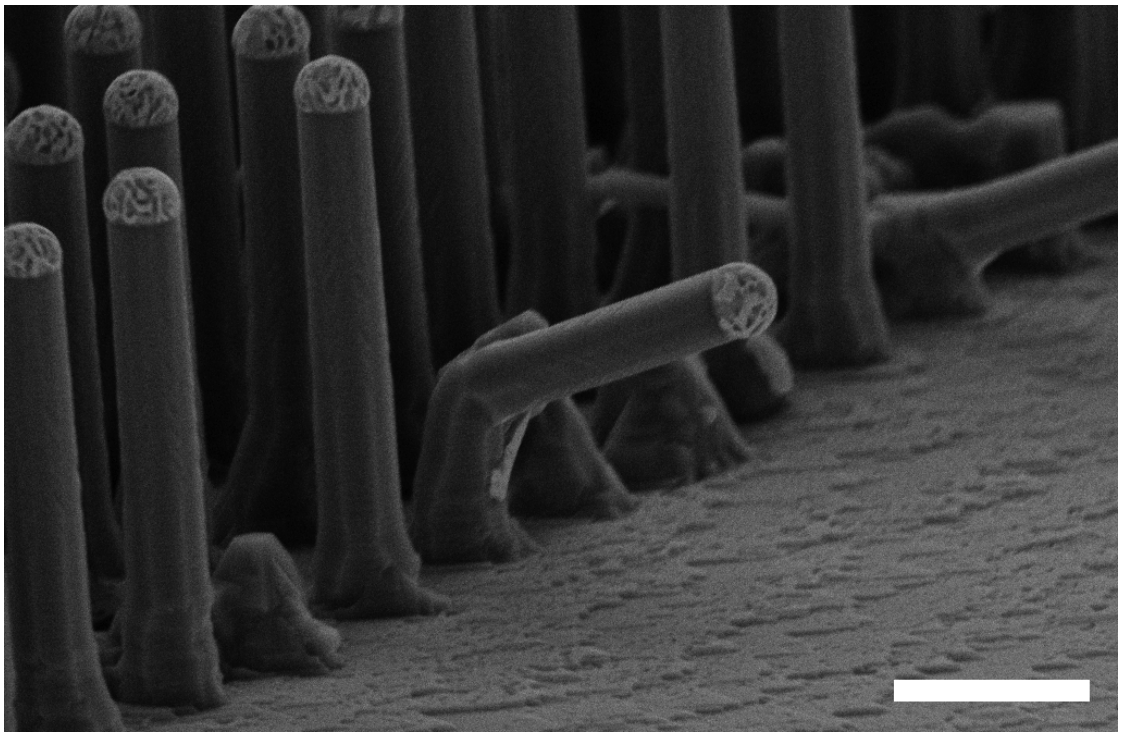

Figure 2.16: The stability of the liquid-solid interface is delicate, significant parameter shifts can disrupt the stability resulting in kinking as seen here. In general this type of defect is reduced by increasing the temperature of the reactor. The scale bar is 2 μm.

Wires approaching micron diameter with arbitrary length and minimal kinking defects are shown in Figure 2.19.

2.8 Single isolated gold catalyzed silicon vapor-liquid-solid wires

Large arrays of wires are needed for large area photovoltaic experiments. Other experiments require individual wires. In some cases it is acceptable to remove wires from their growth substrate to utilize the wires, in others it is vital to leave the wires in place and measure their properties or use the wires in isolation at

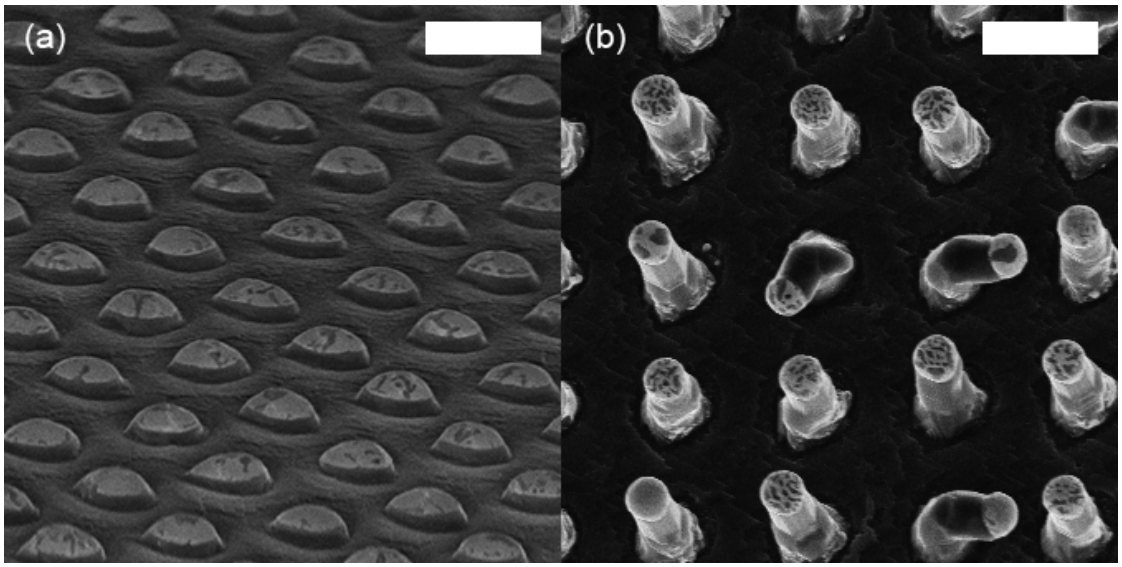

Figure 2.17: Both (a) and (b) were grown at 650 C at 300 mTorr of SiH_4 for 40 minutes. (a) had a flow rate of 10 SCCM and (b) had a flow rate of 40 SCCM. The effect of gas depletion is clear. The partial pressure of SiH_4 in the reactor is clearly low in the first case causing the nucleation and growth rates to be much longer and lower. The scale bars are both 2 μm. (a) is tilted at 80 degrees and (b) is tilted at 20 degrees.

the growth location.

The surface diffusion sinking effect of Au is problematic in this later case when this requirement is combined with the need to create the wire at a well-defined growth location. The growth location can be defined via lithographically defined catalyst; however a single isolated wire growth site results in the maximum surface loss of Au. Thus low density patterns of lithographically defined wires require somewhat different reactor conditions than arrays.

The difficulties in achieving isolated and controlled growth of lithographically defined VLS wires may seem at odds with the ease of growing low densities of wires with colloidal particles and aggregated thin films. The reason such patterns are easy to create in these two other systems are different. In the case of colloidal Au the reason is likely local surface contamination that prevents the

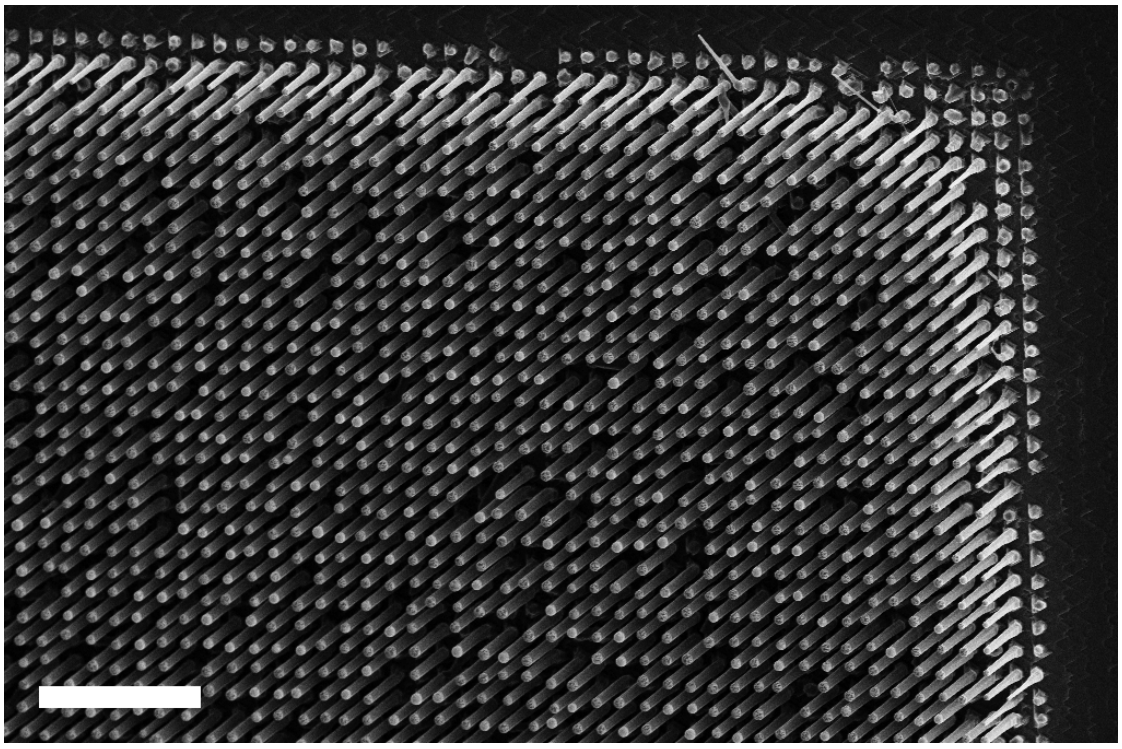

Figure 2.18: The wire sites at the edge of this array are missing due to Au migrating out onto the clean Si surface around the array. The scale bar is 8 μm.

loss of Au to the surrounding surface. In the case of thin film arrogation it is that the surface coverage is already satisfied. The islands that form in such a system are from the Au that is in excess of the needed surface coverage. This observation resulted in experiments in which attempts were made to create samples in which this background coverage was satisfied by a thin film in parallel with lithographically defined catalyst dots. To do this isolated Au was placed at desired growth locations via the standard lithographic method. After the oxide layer was removed as normal, a very thin film of Au was then deposited in the load lock in an attempt to just satisfy the needed surface coverage in the background. This approach ultimately did not work as fine enough control of the background thickness was not possible. Either it was too thin and there was still significant Au loss from the isolated lithographic site or it was too thick and

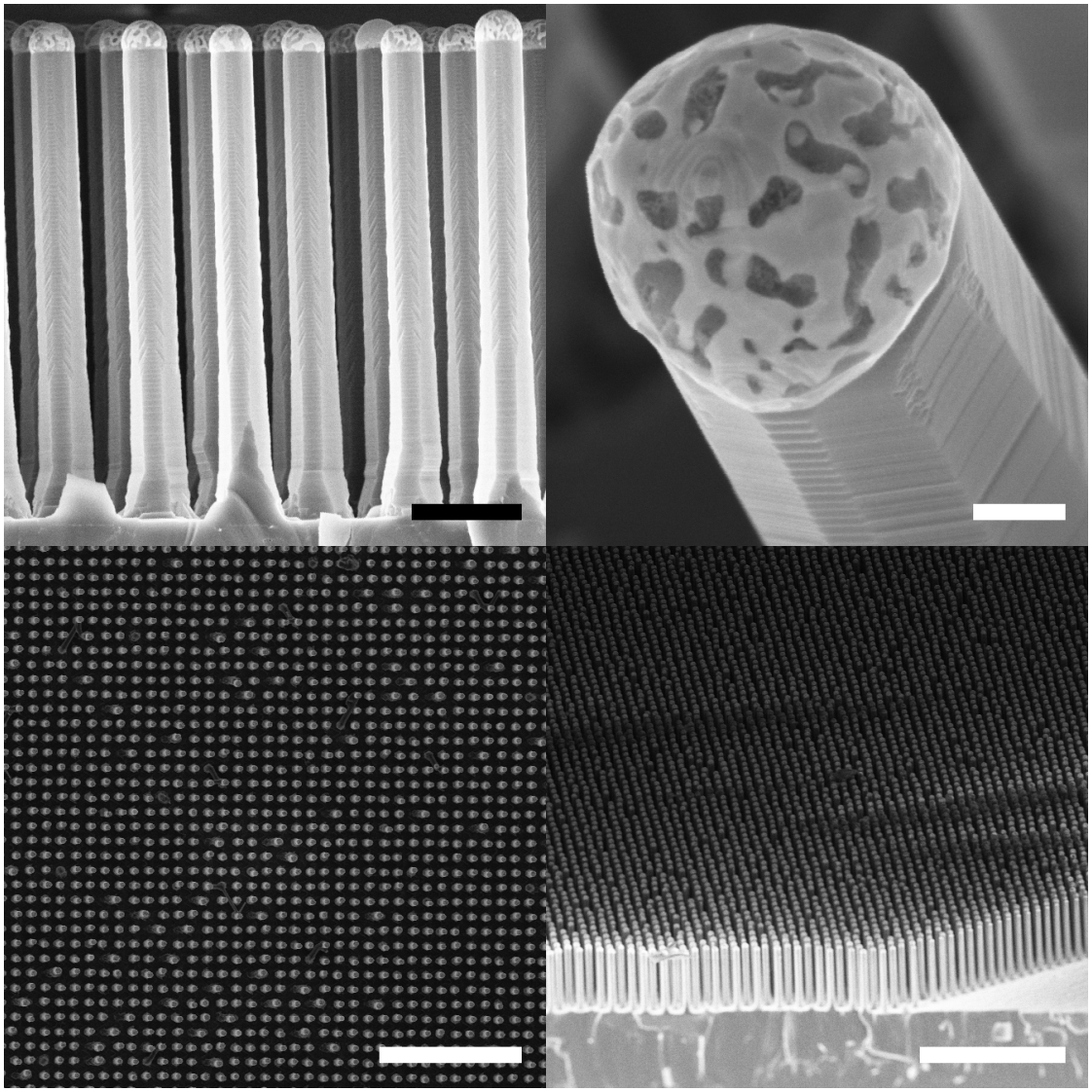

Figure 2.19: Optimized growth parameters allows for the synthesis of large low defect arrays of Si VLS wires. Shown here are several views of such a growth. From the side (90 degrees, upper left; scale bar 2 μm) the facet evolution of the wire is observable. The removal of the wire into the load lock results in a rapid quenching of the catalyst which results in a phase segregation of the Si and Au as seen in the upper right micrograph (scale bar 200 nm). Views from both the top (lower left, scale bar 20 μm) and angle (lower right, scale bar 20 μm) of the array show very low densities of kinking with over 90% of wires growing epitaxially in the <111> direction.

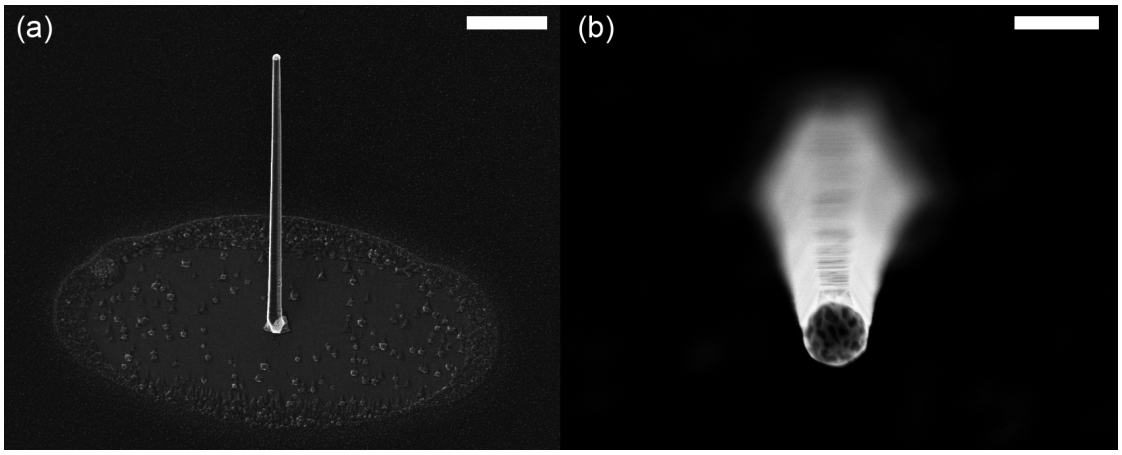

Figure 2.20: Two views of isolated wire growths are shown here. For isolated wire growths Au loss to the surface is a major issue. In (a) this loss is clearly visible as the Au coverage changes the CVD morphology causing a clear nearly circular contrast ring around the Au site. This isolated wire is kinked at the base. In general the lower temperatures needed to grow isolated wires increase kinking over higher temperatures that are usable for type array growths. In (b) a single vertical wire is shown. The scale bars for (a) and (b) are 10 and 1 μm respectively.

islands were formed outside the lithographic site from which extra undesired wires grew.

Ultimately the solution to growing isolated VLS wires from lithographically defined Au was simply to reduce the temperature (slowing the surface diffusion rate) and increase the amount of Au at the lithographic site with the expectation of some loss. This combination permits a very small VLS CVD window that is able to grow isolated lithographic VLS wires (Figure 2.20). At low temperatures fragmentation of the site is as normal an issue, as the temperature increases a single often kinked wire is grown. At the maximal temperature in the window the kinking effect is suppressed enough that yields are as high as 50%. This high yield window of epitaxial isolated Au catalyzed VLS wires is small around 600 C. An increase in temperature of 15 C will yield no wires at all; the Au will be lost to the surface. A decrease in temperature of 15 C will yield a high rate of

kinking defects. Standard parameters for growing an isolated VLS wire from Au are an Au evaporation thickness of 80 nm in a 1 μm diameter well. The Au is annealed at 600 C in UHV for 5 minutes then grown at 600 C in pure SiH_4 at a pressure of 250 mTorr for as long as needed, typically 20-30 minutes.

2.9 Aluminum catalyzed silicon vapor-liquid-solid wires

Growth of Al catalyzed wires requires the use of a UHV reactor. Any exposure to oxygen creates an alumina shell on the Al which prevents VLS from occurring. Because of this only in-situ evaporation in the CVD reactor is possible for depositing the needed catalyst. This limits the growth of Al wires to methods which are based on blanket deposition of a thin film. This in turn limits both the size and density of Al catalyzed wires. Creation of these materials depends on the UHV load lock evaporator in the IBM reactor. In general blank Si <111> wafers were used. After being cleaned and dipped in HF the wafers or chips were placed in the load lock and pumped overnight to a pressure less than 0.1 μTorr. At this pressure 6-9 nm of Al was deposited and the sample transferred into the reactor where it was annealed under UHV. Typically this anneal was 20 minutes in duration with temperature controlling the desired island size and wire diameter. The largest wires ($d \approx 200$ nm) created by this method were formed using an anneal temperature of 750 C. The growth after the anneal was typically carried out at a pressure of 550 mTorr with SiH_4 at 490 C (Figure 2.21). The time controlled the length of the resulting wires.

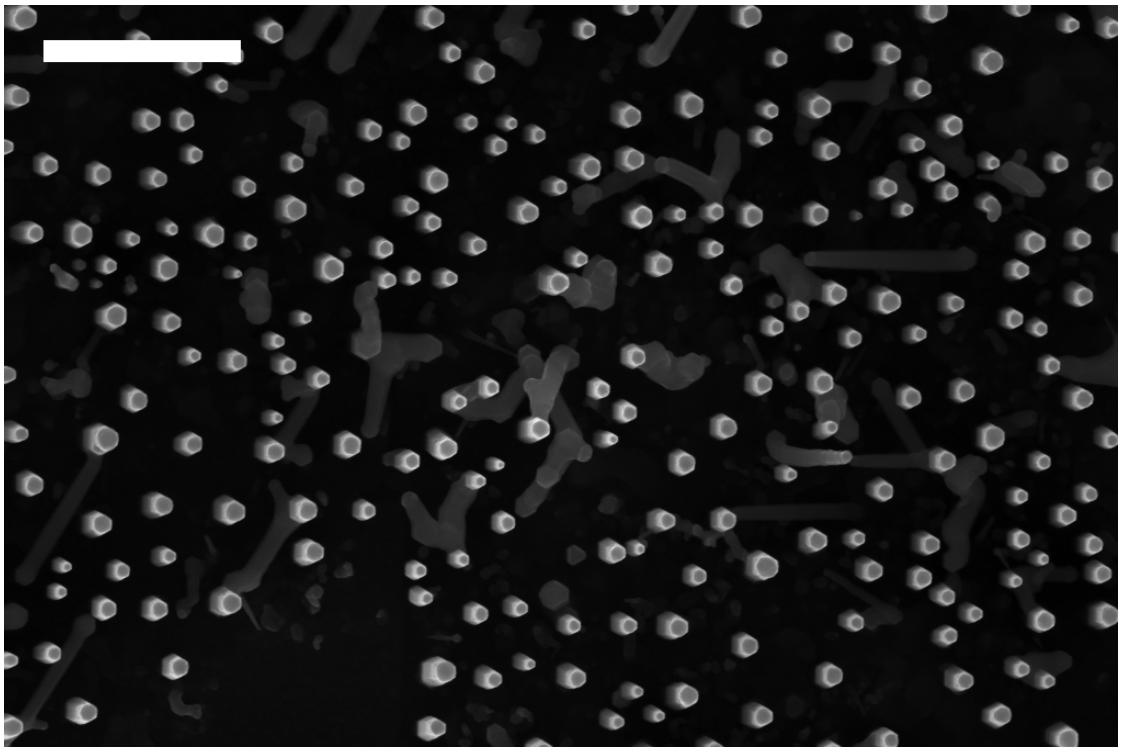

Figure 2.21: Growth of Al catalyzed Si wires proceeds from thin films deposited in-situ in the UHV reactor. These growths share characteristics with synthesis based on aggregated Au films in that they have a spread in the wire diameter. Here the majority of wires are vertically oriented. The scale bar is 1 μm.

2.10 Summary

VLS growth is a complex with material science that remains an area of study today. I was able to grow Ge wires directly on Ti films using Au as the catalyst in both the Park and IBM reactors. Studies of other metal-metal-semiconductor growth systems did not yield crystalline materials. The VLS growth parameter space for Si wires using Au catalyst was explored extensively enabling both high density and isolated growths. Large diameter VLS wires require higher temperatures to remain free of orientation defects and fragmentation. Al catalyzed Si wires are limited by the requirement of in-situ evaporation of the catalyst material.

CHAPTER 3

TRANSMISSION ELECTRON MICROSCOPY OF GERMANIUM NANOWIRES

3.1 Introduction

Transmission electron microscopy (TEM) is a vital tool for inspecting nanoscopic materials. TEM technique is somewhat more involved to learn than other common microscopy such as atomic force microscopy (AFM) or scanning electron microscopy (SEM). A significant fraction of the difficulty in conducting TEM work is contained in sample preparation. While samples for AFM and SEM generally are used without modification samples for TEM rarely are. This is because TEM samples must be electron transparent. TEM specialists have several general purpose techniques to produce these thin samples. In this chapter the application of these methods will be commented upon with respect to nanowire TEM and a new technique will be introduced that enables efficient observation of nanowire specimens.

3.2 Membrane and other support grids

For Si at 200 keV the onset of electron transparency is on the order of 100 nm in thickness. In general for TEM the thinner the specimen the better the imaging will be. For scanning transmission electron microscopy (STEM) very thin samples are essential. The requirement of 100 nm thickness is intrinsically achievable with VLS nanowires. Growth of nanowires with diameters around 20-30

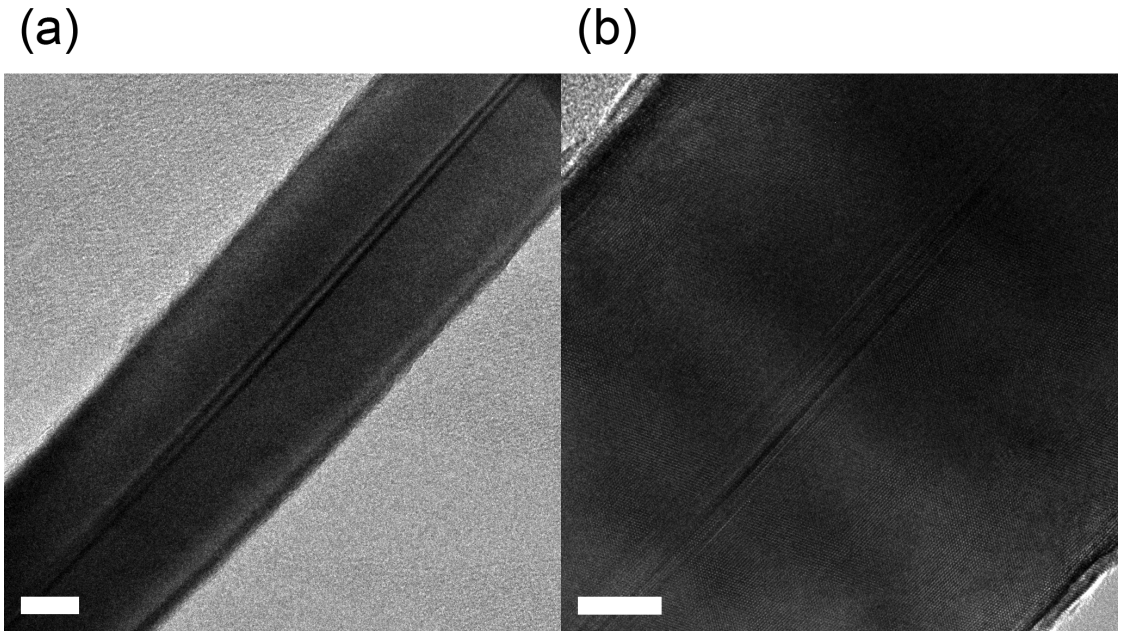

Figure 3.1: An 80 nm Ge nanowire with a twin plane defect is shown. The wire was removed mechanically onto a carbon membrane grid to make this bright field TEM observation. Both (a) and (b) show the same wire. The scale bar of (a) and (b) are 20 nm and 10 nm respectively.

nm are perhaps the easiest of all syntheses to achieve. Therefore it is common to see nanowires removed from their growth substrate and onto a membrane or other type of support grid such as a bar grid to perform TEM. The grid serves as the microscope slide in TEM and in the case of mechanical removal of already electron transparent nanowires allows for quick sample preparation. In this method wires are either mechanically brushed off onto the grid or are removed into a liquid such as isopropyl alcohol and this fluid containing nanowires is dried on the grid. In both cases the result is a electron transparent nanowire suspended on an electron transparent support. I used this method to make my first TEM observations of nanowires (Figure 3.1).

The attraction to this method for nanowire preparation is clear in that it is simple and fast and allows observation of the nanowire material quality in the

upper section of the wire without encapsulation or damage. The principle disadvantages of this method with respect to nanowires is that it does not allow for the observation of the substrate/wire interface because the wire is fractured above this point. Additionally the support membranes of the grid can sometimes break due to local heating caused by the TEM beam.

3.3 Wedge polishing

Another common TEM preparation technique is wedge polishing. This method was primarily invented for thin film specimens. In this method two halves of the same sample are glued with a strong adhesive (M-Bond 610) face to face after being cut with a diamond wire saw in the desired crystal direction. This material is attached to a very flat chuck and polished against an abrasive pad. These pads can have different abrasive agents but for my work diamond was used exclusively. The material is polished using progressively smaller diamonds until a flat mirror finish results and the sample thickness is on the order of 100s of μm thick (the choice of which depends on the next step). This thin material is removed and glued to a polished optical flat which is then tilted at an angle with respect to the abrasive pad. This angle is transferred to the sample resulting in a wedge shape. Interference colors on the optical flat allows observation of when the sample is thin. After the mechanical polishing is complete the sample is often thinned further in a low angle Ar ion mill. The end result of these processes is a wedge that has an end which is thin enough for the TEM beam to pass through. This type of sample also has thicker material available which can be extremely helpful for aligning the microscope for lattice resolved imaging.

This method is ideal for uniform thin films. For nanowires it affords the opportunity to see the wire/substrate growth interface in principle. However there are several problems with its application to nanowire materials. The method relies on the mechanical stability of the sample being polished. This is achieved in thin film samples with a thin layer of epoxy between the two halves, a thin so called glue line. For nanowires the glue line cannot be thinner than the height of the wires being observed. This results in samples with a much wider glue line than is typical in the thin film case which makes the final ion milling poor (the glue mills at a different rate than the substrate) and has compromised mechanical stability. This can result in the disintegration of a sample while polishing. Given that complete polishing of such a sample can take a novice up to 6 hours this is an issue of significance.

The other major issue with using this method for nanowire samples is specific to nanowire samples grown at low density for instance from colloidal catalysts. In these systems the probability of a nanowire being in the transparent portion of the wedge is low. This results in the majority of samples not containing any wires in the most desirable part of the sample.

I applied this method and having encountered these issues decided this method while recommended by the microscopy community at Cornell was not an effective means of studying nanowires.

3.4 Focus ion beam milling

As just alluded to at the time this TEM work was being undertaken the nanowire samples were being grown from colloidal catalysts and the sub-

strate/wire interface was of interest. Taken together these requirements removed wedge polishing and membrane based grids from consideration. Focused ion beam (FIB) milling allows precise removal of material on a nanometer scale using a beam of heavy ions, commonly gallium. This process is used industrially to examine failed circuits and has been applied to TEM sample preparation.

The ability to observe the area from which the TEM sample will be created with a SEM in parallel to the ion beam resolves the density related issue that plagued wedge polishing. However this method is still created with planar structures in mind. The FIB beam causes damage particularly at high voltages (30 keV) and so the top surface of planar structures are commonly coated in a layer of Pt. Application of this protective layer is not possible for nanowire structures. In addition their extruded nature results in redeposition effects (Figure 3.2) that creates additional problems for making an electron transparent specimen from substrate to tip.

Taken together these issues make FIB based preparation non-optimal for creation of nanowire TEM specimens.

3.5 Double ridge method

Having confronted the aforementioned issues with traditional TEM preparation techniques I decided to create my own method tailored to the nanowire samples I wished to observe. The experience of attempting the traditional techniques enabled me to know what was needed to create a good TEM specimen. Clean room experience provided the needed skills to create a better method.

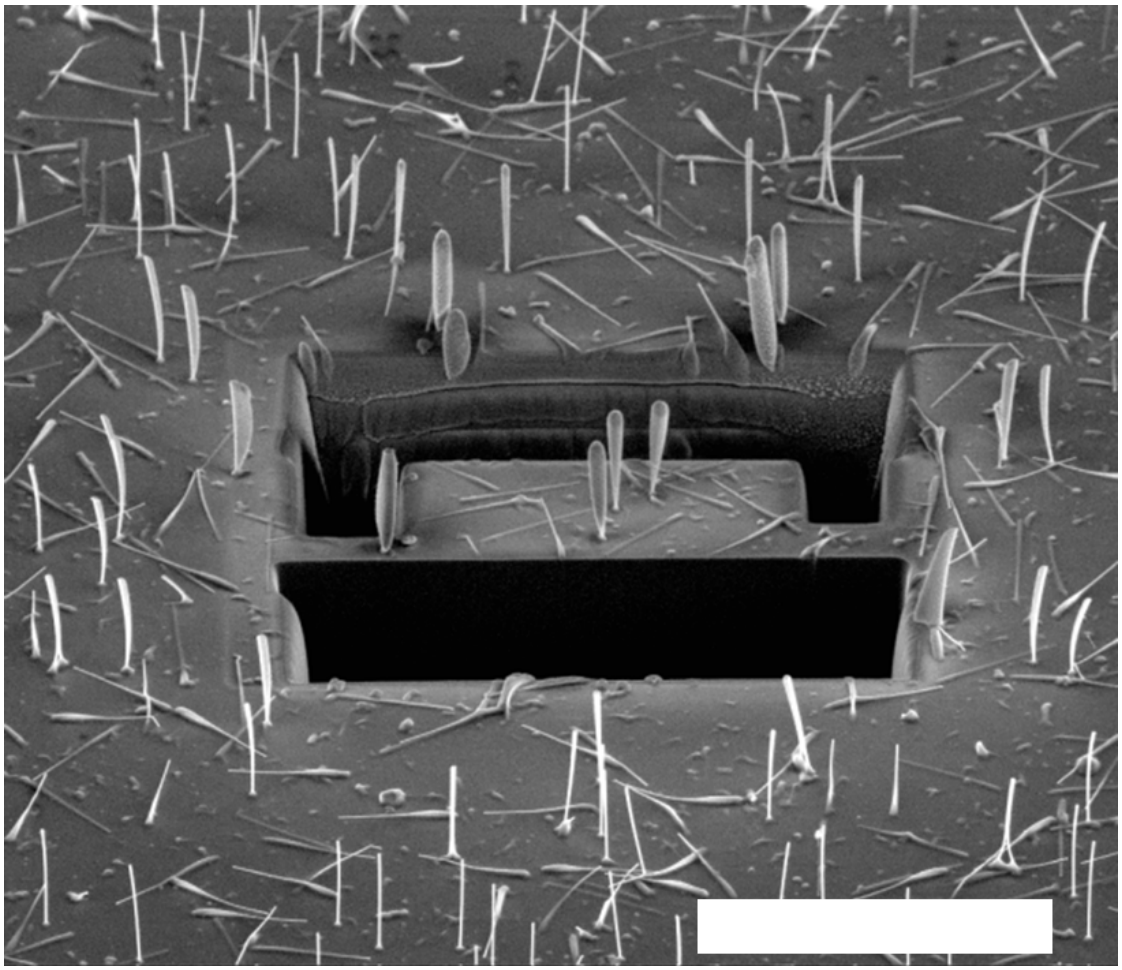

Figure 3.2: Creation of nanowire TEM samples via FIB milling is difficult both because of damage, seen as wilting, and deposition effects. The scale bar is 20 μm.

I wished to study via TEM the Ti-Au-Ge nanowire system which was effective in growing straight Ge nanowires on metallic thin films. In particular I wanted to see if there was any interaction at the substrate/wire interface between the 3 materials. In this system the nanowires themselves could be grown intrinsically electron transparent with a diameter of nominally 40 nm. Therefore all that was needed to study the substrate/wire interface was a substrate that was already compatible with TEM.

Such a substrate was achieved by the following means. A <111> silicon

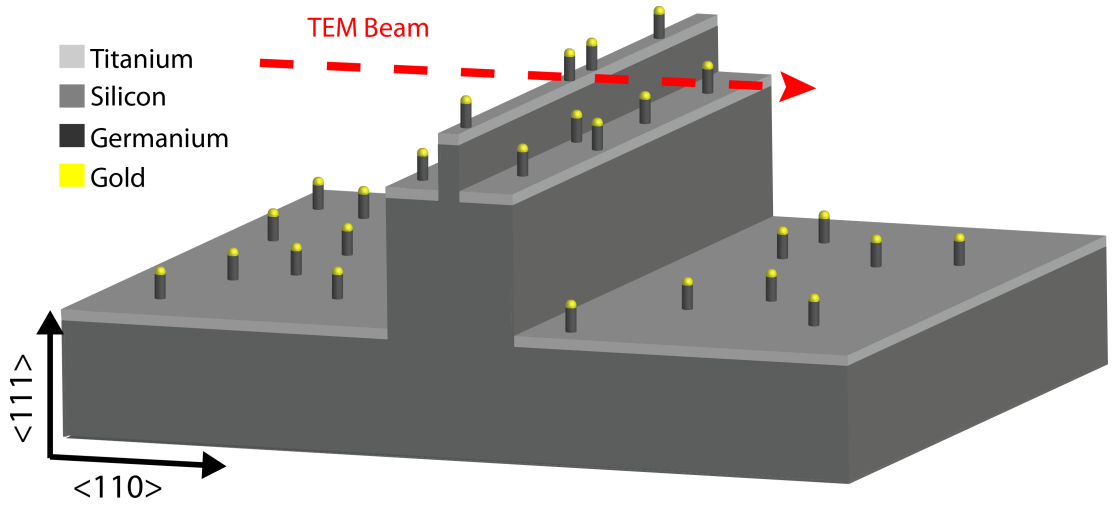

Figure 3.3: Schematic showing the double ridge structure, not to scale. The minor ridge is ≈ 100 nm × 1 μm, the major ridge is 40 μm × 40 μm, and the supporting wafer is 250 μm wide. The structure is made from a <111> Si wafer and the ridge is oriented so that the <110> direction is perpendicular to the ridge.

wafer was sourced and a set of lines defined via lithography perpendicular to the <110> direction in resist. These lines were isolated allowing for significant overexposure of the resist. This combined with exploitation of the small non-ideal isotropic component of a CF_4 RIE allowed the definition of a small ridge ≈ 100 nm x 1 μm. I refer to this ridge as the minor ridge. Following the RIE the resist was removed and the wafer recoated in a second lithographic step to define another wider ridge with the minor ridge at its center. This major ridge was 40 μm wide etched using Bosch RIE to a depth of 40 μm. This double ridge pair was then diced parallel to the ridges into 250 μm wide strips with each strip containing one double ridge structure (Figure 3.3).

To study the Ti-Au-Ge system Ti was evaporated onto this structure to a thickness of 25 nm and 40 nm Au colloids deposited as the catalytic material for VLS of Ge nanowires.

The structure described meets the requirements of TEM. The substrate is the double ridge structure with the viewable area being the top of the minor ridge. Although this area seems very small it is very large compared to the viewable area of a wedge polished or FIB milled sample. As described the transparent area extends the full width (several mm) of the TEM column at equal thinness. Contrasting this with an aggressive 1 degree wedge polish which has a viewable length of nominally 5 μm the advantage of this method for low density nanowire growth is clear. In addition after fabrication of a wafer of ridges the sample preparation time is very small. When compared to FIB preparation this method is notably free of damage to the nanostructures.

Although only the minor ridge is needed to provide electron transparency the major ridge is required to allow for tilt in TEM in the direction perpendicular to the long axis of the ridges. In this direction the described structure allows for tilt of up to 2.8 degrees. Tilt in the direction orthogonal to the ridge is limited only by the microscope.

The alignment of the ridge perpendicular to the <110> direction allows for easy calibration of the microscope with these samples. It also allows assessment of epitaxial registry in samples were such registry is possible.

3.6 Transmission electron microscopy observations of the Ti-Au-Ge system

I used the method described in the previous section to study Ge VLS nanowires grown from 40 nm Au colloids on a 25 nm Ti thin film. These wires were grown

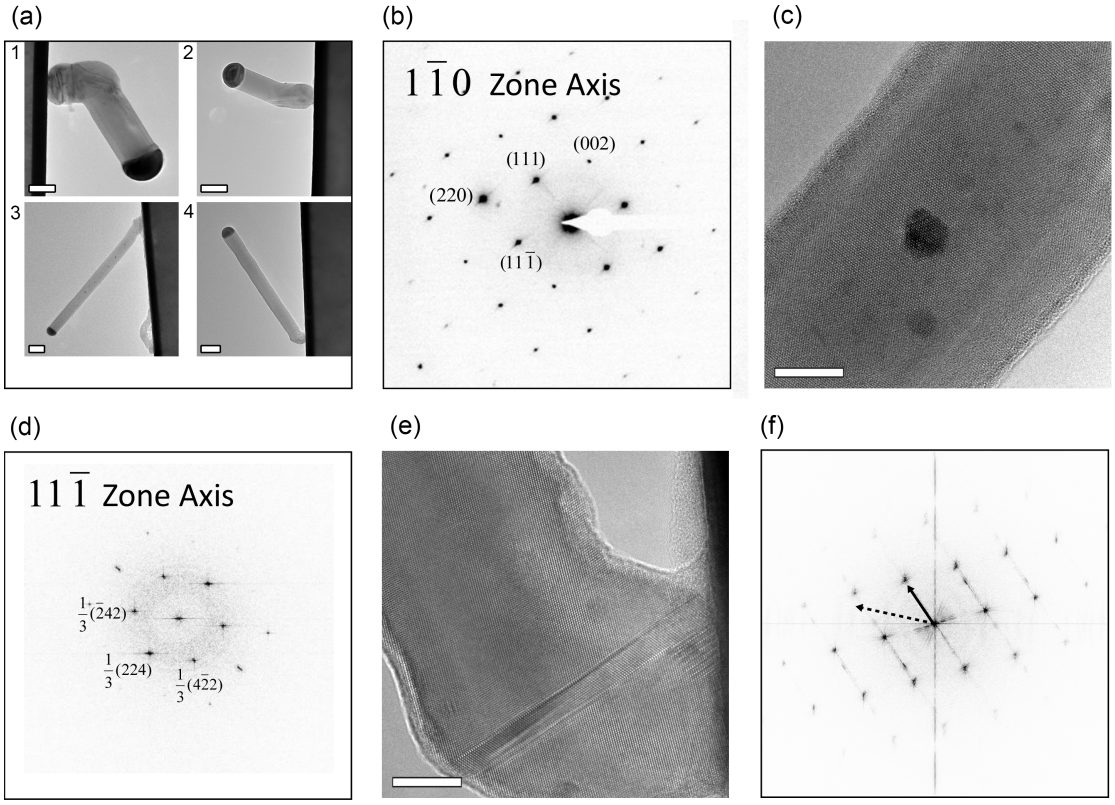

Figure 3.4: (a) 4 examples of nanowires with kinks at the boundary between defective and defect free regions; (b) selected area diffraction (SAD) indexing of the nanowire in [a4, e] showing <111> growth direction; (c) HM-TEM showing a sidewall bumps (dark areas), two side facets (edges) and low defect central area; (d) FFT indexing of wire in [c] showing <112> growth direction; (e) HM-TEM showing the base of wire in [a4] exhibiting defects and change in growth direction; (f) FFT of [e], the dashed arrow indicates the initial growth direction as seen in [e] which is not in any low order direction, the solid arrow indicates the final growth in the <111> direction. The scale bars for (a), (e) and (e) are 50, 10 and 10 nm respectively.

in the Park group reactor described in chapter 2. Synthesis of the Ge nanowires was carried out in an atmosphere of GeH_4:H_2. The total pressure was 100 Torr and the GeH_4 partial pressure was 1.5 Torr. The colloids were deposited on the Ti film after treatment with poly-L-lysine (0.1% w/v). Optimal growth occurred between 310 and 330 C.

HM-TEM observations of 40 nm Ge wires on Ti show several interesting

features. The nanowires did not grow in any preferred direction relative to the substrate which is reasonable given the amorphous nature of the Ti film. All observed 40 nm wires were strongly faceted single crystals growing in either the <111> or <112> direction (Figure 3.4b,d). Observation of diffraction peaks in the <112> direction are forbidden by the structure factor in a bulk crystal however for these finite nanowires the small thickness variation of the faceted surface allows the observation of fractional 1/3 {224} reflections [24] which have been previously seen in similarly sized Si nanowires [25]. The nanowire side facets were flat with only a small amount of uncatalyzed CVD growth occurring in the form of small hemispherical bumps on the side wall surfaces. These appear as contrast dots in HM-TEM (Figure 3.4c) due to their lattice orientation mismatch with the underlying wire and are more readily identified as bumps via scanning transmission electron microscopy (STEM, Figure 3.5a). The wires did not exhibit the initial diameter taper of epitaxially grown wires [26]. This implies that the Au-Ge eutectic has a contact angle greater than 90 degrees to the growth surface. This growth surface is at least initially a thin amorphous TiO_2 layer created by the exposure of the Ti film to air. It is notable that pure Au has a nominal contact angle of 122 degrees to (110) TiO_2 [27] thus the observed lack of wetting is not entirely surprising.

Nearly all nanowires observed consist of two parts: an upper nearly defect free region and a defective region near the Ti thin film that is comparable in size to the catalyst diameter. This defective region consists of one or more grains that merge into a single crystal wire. The transition between the defective region and the low defect region is marked by a change in the growth direction of the nanowire or 'kink' (Figure 3.4a). Although the wire changes growth directions the crystal orientation relative to the substrate does not change at the

kink. A variety of mechanisms can cause nanowires to kink [28] [29]. In the wires under observation kinking is needed to allow the nanowire to grow in the energetically favorable [19] <111> and <112> directions (Figure 3.4e,f). These directions have the lowest surface energy in a diamond lattice [30]. Although surface tension and other terms change the energy balance of the liquid-solid interface at the size of the wires under study the surface energy term dominates and so the two aforementioned directions are preferred. The reason why the <111> and <112> surfaces have the lowest energy follows intuitively from the surface energy being directly proportional to the number of dangling bonds on a surface [31].

These observations suggest that at the amorphous Ti surface there is no preferred direction for nucleation, so a randomly oriented crystal initially precipitates. As the growth of the crystal continues the catalyst moves to the nearest energetically favorable facet. This movement combined with the continual growth of the crystal forms the kink. Once the catalyst reaches the energetically favorable facet the wire growth proceeds as it would on a matched wafer: as a low defect single crystal. Some nanowires also contain kinks far away from the base region. These kinks do not serve as boundaries between defective and defect free regions of the wire and are likely caused by another mechanism, such as motion in the position of the catalyst meniscus caused by a variation in the process parameters that disturbed the delicate balance of surface tension at the wire tip.

The nanowires are not tapered. Given the lack of sidewall growth this implies that there is no major Au migration or incorporation in the nanowires. EELS measurements of both the central wire and sidewall bumps show no de-

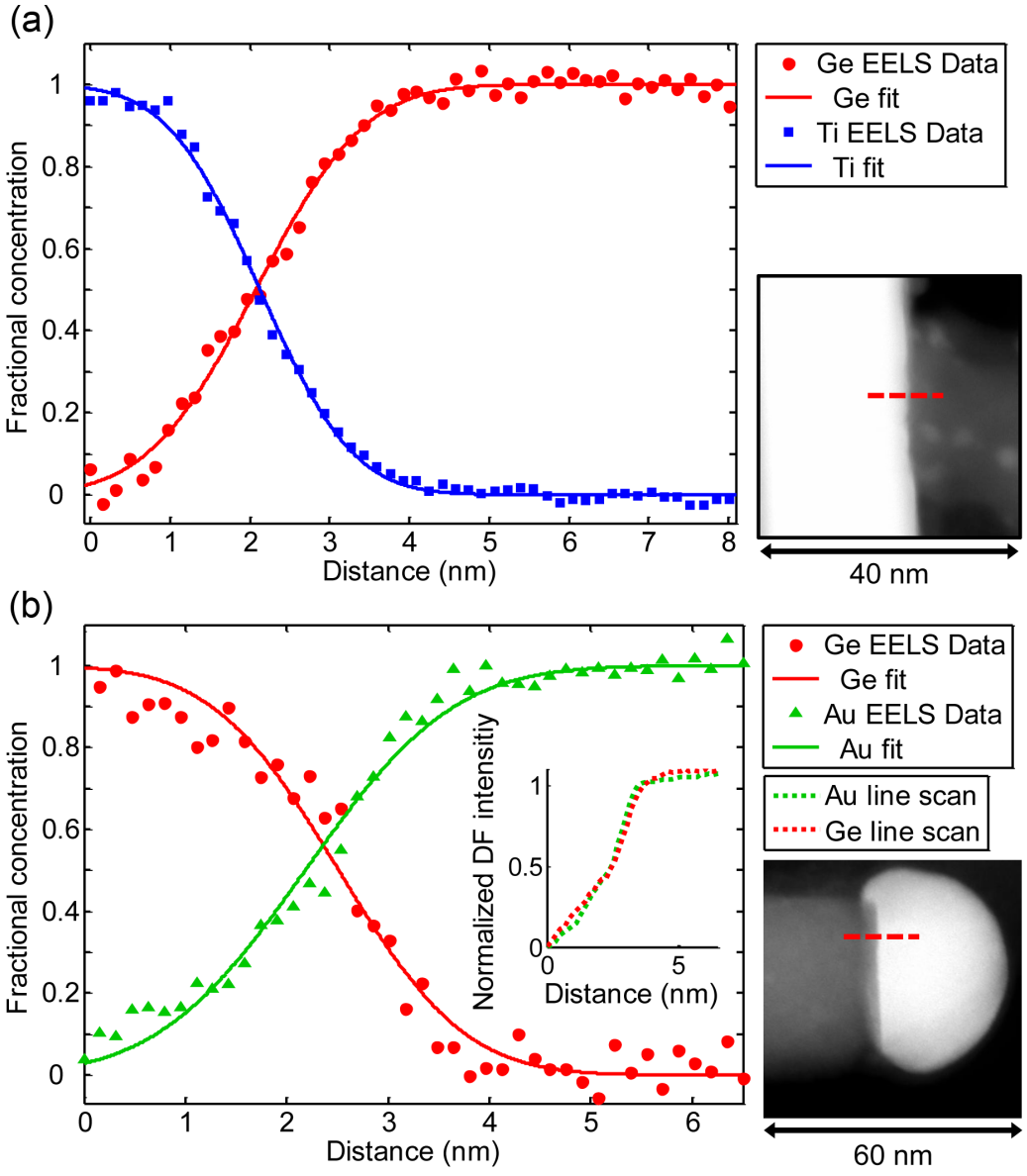

Figure 3.5: EELS line scans of top and bottom wire/metal interfaces with data fitted to complementary error functions, the dashed line in the STEM images shown at right indicate the position of the line scans. (a) Ti/Ge interface (spectrometer dispersion 0.5 eV/channel); (b) Au/Ge interface (spectrometer dispersion 0.3 eV/channel). The Au/Ge interface data was collected with two line scans due to the large energy separation of the EELS edges. The inset (b) DF intensity shows the alignment of the two scans compensated for drift. The composition does not cross at 0.5 due to imperfect drift correction.

tectable Ti or Au signals implying that the bumps are uncatalyzed growths which may simply nucleate on point defects in the crystal's sidewall.

EELS line scans of both the top and bottom metal/wire interfaces were also performed. The EELS data is consistent with a Gaussian beam with a standard deviation of ≈ 1 nm sweeping over an atomically sharp interface and places an upper bound on the transition width (10-90%) of the Ti-Ge and Ge-Au interfaces of 2.4 nm and 2.9 nm respectively (Figure 3.5). The Ti film is an order of magnitude thicker than this upper bound implying the thin film can be treated as identical to bulk. This minimal alloying is consistent with expectations [32] given the relatively low temperature (310-330 C) and short growth time (< 10 minutes) used. This weak interaction is an important feature. If the rate of germanide formation had exceeded the wire growth rate the resulting structure would simply have been a germanide of little use. Because the reverse is true a two step process is possible: first grow the wires and second form the germanide needed for a low contact resistance.

Energy dispersive X-ray measurements (EDX) of the lithographically prepared samples show no detectable elemental contamination from processing (Figure 3.6). SEM observations show that the same morphologies are present on all sample types. Ge nanowires grown on Ti films are of comparable structural quality to Si control samples grown simultaneously. These control samples do not exhibit epitaxy due to the low temperatures used (below the Au-Si eutectic point).

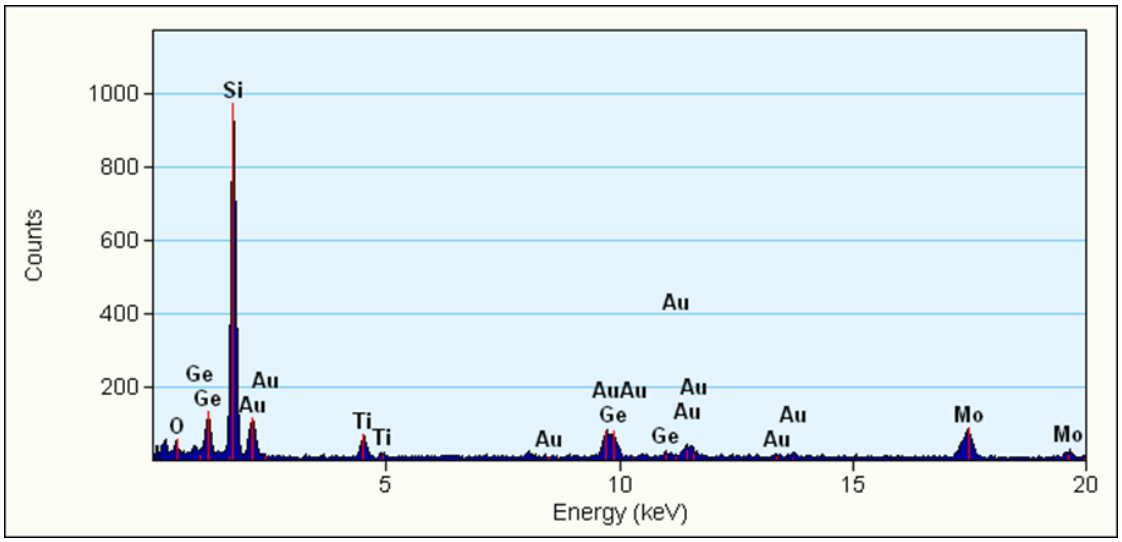

Figure 3.6: EDX data taken on a double ridge Ti-Au-Ge sample shows only the expected materials. Mo is in the system because the slot grid on which the double ridge is glued is made of Mo.

3.7 Summary

Ge nanowires catalyzed via Au grown on Ti films are observed to be of comparable quality to controls grown on Si. These wires are low defect single crystals that grow in directions which minimize the free energy of the liquid-solid interface. A kink near the base of the wire/substrate interface is common to most observed wires and is the result of the catalyst moving to the needed direction that will minimize the interfacial free energy. The Ti-Au-Ge results in minimal alloying at both metal-semiconductor interfaces as measured by EELS. This result is likely made possible by TiO_2 on the metal surface which is not reduced at the reactor conditions used. The double ridge method introduced offers more rapid and complete observation of VLS nanowires that are intrinsically electron transparent than traditional TEM sample preparation techniques.

CHAPTER 4

SEMICONDUCTOR WIRE PHOTOVOLTAICS

4.1 Introduction

The primary theme of this thesis is research related to applying VLS wires as photovoltaics. In chapter 1 this topic was placed in a greater social, engineering and economic context. In this chapter the benefits and deficiencies of applying VLS wires as photovoltaics are discussed and measurements of VLS and control photovoltaics cells are presented.

4.2 Photovoltaics background

To make these advantages and disadvantages clear it is helpful to first review some basic physics of how conventional semiconductor photovoltaics work. An excellent general review of this material can be found in the Handbook of Photovoltaic Science and Engineering [33], a voluminous reference on conventional and emerging photovoltaics.

Solar cells come in many flavors. Here I will focus just on photovoltaics, systems that directly convert light into electricity. Even among photovoltaics there is great diversity. However that diversity can be broken down into two major classes, photovoltaics that operate with thermalized carriers and those that have hot carrier effects.

When a photon strikes a semiconductor its energy can be absorbed by an

electron. If this happens it excites the electron above its ground state. There are many ways to look at this excited state depending on what simplifications you want to make to the system. For photovoltaic purposes all that matters when a photon is absorbed is if it frees and an electron from an atom or it does not. This atomistic view, while true, is not the most helpful though. Typically semiconductors are parameterized into band structure that describes the dispersion of electrons and their quasi anti-particle holes. In this parlance when a photon is absorbed it creates an excited bound state called an exciton. This bound state can be broken apart by various means such as an electric field or thermal energy (in particle terms phonon absorption). It also can recombine giving up the photon's energy to the host crystal (phonon), to another atomic particle, by reemitting a photon or a combination.

Recently there have been many interesting experiments showing that some materials have so-called multi-exciton generation [34]. In these materials a single excited exciton can be viewed as generating additional excitons by means of photons rather than thermalizing via a phonon. Together with materials that allow for carriers above the band edge to reach the boundaries of the system (i.e. the contacts), I classify these systems as hot carrier photovoltaics as they extract energy above the bandgap of the material into more coherent forms of energy than heat. Materials with hot carrier effects currently work under very limited conditions.

Most photovoltaics are not like these hot carrier materials. In most photovoltaics the carriers can be considered to be in thermal equilibrium at all times. In these systems if the exciton created by the photon is broken apart then the disassociated electron and hole are quickly thermalized in the phonon bath of

the material. For this reason historically photons are normally said to generate electron-hole pairs (EHP) in semiconductors rather than excitons. Though such a state has to exist it is so easily dissociated in conventional bulk semiconductors that in essence an electron and hole are always created and relax to the band edge immediately. In indirect semiconductors absorption of photons is not strong because it is a two particle process quantum mechanically requiring both a photon and a phonon. In indirect semiconductors the small matrix element for photon absorption means an equally small matrix element for direct recombination (photon emission). This partially offsets the poor absorption in indirect semiconductors by generally giving them higher carrier lifetimes than their direct bandgap counterparts. In this thesis only indirect bandgap semiconductors (Si and Ge) are used.

The goal of any photovoltaic cell is to make the best possible use of incoming photons. This problem has two basic parts: absorbing as many photons as possible, and collecting as many carriers as possible. Nano and microstructure materials including VLS wires offer opportunities and challenges in both parts.

To see the opportunities and challenges it is helpful to look at the operation of a simple *pn* homojunction photovoltaic. The band picture of this junction is shown in Figure 4.1. There are three regions of interest in this picture in terms of photovoltaic action, an EHP created in the depletion region, near the depletion region, and far away from the depletion region. To get photovoltaic energy out of the system the carriers created must disturb the equilibrium carrier densities. If the carrier densities are changed then so too are the quasi-Fermi levels which shows up externally to the cell as a voltage.

Now consider what occurs if an EHP is created in each area. First consider

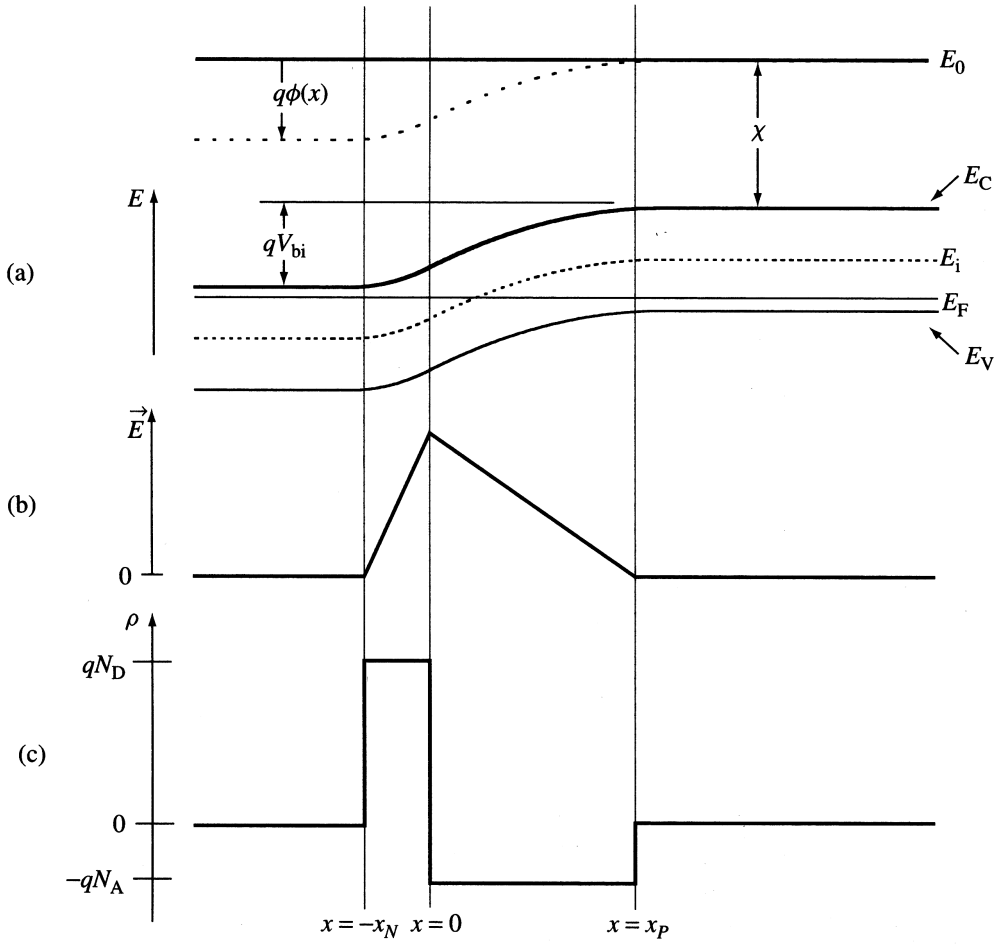

Figure 4.1: Figure 3.14 from [33], showing a *pn* junction in equilibrium. The band structure (a), electric field (b), and charge density (c) are illustrated.

far away from the depletion region on the n side of the junction (the p side simply swaps the minority/majority carrier type). In this case there is one extra electron and one extra hole. In this region there is no driving field to separate the electron and hole and because both carrier types have equal excess the carriers will simply recombine after some time. Thus in general a photon absorbed far away from the junction is wasted.

Next consider a photon absorbed in the depletion region. In this area there is an electric field from the exposed positive charge on the n side and exposed

negative charge on the *p* side. In equilibrium the field or drift current is balanced in the junction with the diffusion current. Another way of looking at the *pn* junction is that a field arises which exactly offsets the chemical potential that drives the diffusion process. Thus the field stops extra electrons from leaving the *n* side and extra holes from leaving the *p* side. When an EHP is created in the depletion region it is separated by the field with each carrier ending up on the side where they are the majority carriers. Once to the opposing side they are essentially safe because there are few minority carriers available to recombine with them. This results in the desired excess carrier densities in the cell that creates usable electricity.

Last consider when a photon is created near the depletion region on the *n* side of the junction. In this case the electron is where it needs to be as seen from the previous case but the hole is not. If the hole is close to the junction it may diffuse a great enough distance before recombining that it reaches the edge of the field region. If this happens the field will sweep it across the depletion region. The distance over which the carrier can diffuse depends both on the carrier mobility and lifetime. In bulk planar Si *pn* junction photovoltaics this mechanism is the dominant contribution to the photocurrent. For this reason *p*-type substrates are generally used to allow the electron with its higher mobility to be the minority carrier.

The preceding qualitative discussion already contains much of the information needed to optimize a photovoltaic cell. To be more quantitative the system has to be described in more detail. Physically the typical approximations that are made to allow for simple to understand solutions are the same as those used to solve for transport in the classic *pn* homojunction diode. As this material is

likely familiar to the reader and is lengthy it will not be repeated in full here. I will however highlight some important results from the derivation found in the Handbook of Photovoltaic Science and Engineering [33].

In the qualitative discussion I noted that in most *pn* junction photovoltaics the term which contributes the most power is the diffusion of minority carriers to the edge of the junction. In low level injection the dominance of this term means that the transport of these carriers is what is typically solved for via the minority-carrier diffusion equations. The solution to this problem with light injected carriers is:

$$I = I_{SC} - I_{o1}(e^{qV/kT} - 1) - I_{o2}(e^{qV/2kT} - 1) \tag{4.1}$$

This equation is the most commonly used model for a *pn* junction photovoltaic cell. The first term I_{sc} represents the extractable current under short circuit conditions. This current is twice the absorbed photon count less any recombination that has occurred before the carriers reach the contacts.

The second term is the conventional diode equation. The important device dependent physics is contained in the prefactor $I_{o1} = I_{o1,p} + I_{o1,n}$:

$$I_{o1,p} = qA\frac{n_i^2}{N_D}\frac{D_p}{L_p}\frac{D_p/L_p \sinh((W_N - x_N)/L_p) + S_p \cosh((W_N - x_N)/L_p)}{D_p/L_p \cosh((W_N - x_N)/L_p) + S_p \sinh((W_N - x_N)/L_p)} \tag{4.2}$$

$$I_{o1,n} = qA\frac{n_i^2}{N_A}\frac{D_n}{L_n}\frac{D_n/L_n \sinh((W_P - x_P)/L_n) + S_n \cosh((W_P - x_P)/L_n)}{D_n/L_n \cosh((W_P - x_P)/L_n) + S_n \sinh((W_P - x_P)/L_n)} \tag{4.3}$$

Here A is the junction area, N is the doping density, L is the carrier diffusion length ($L = \sqrt{D\tau}$), D is the diffusivity, W is the bias dependent depletion length, x_p, x_n are the bias free depletion lengths, S is the surface recombination velocity, and n_i is the intrinsic carrier density.

This prefactor represents the dark current in the device and is caused by

recombination in the quasi-neutral regions of the diode. If there is no recombination the minority carrier diffusion length goes to infinity and the dark current goes to zero. The important items to note for designing a photovoltaic cell are all in scaling. Consider the dimensional part of the prefactor of the n-type side $\frac{qAn_i^2 D_p}{N_D L_p}$ this can be rewritten in terms of the more fundamental mobility and lifetime of the material as $\frac{Ani^2}{N_D}\sqrt{\frac{kTq\mu_p}{\tau_p}}$. From this formulation we see that the dark current is proportional to the junction area, scales inversely with doping and is improved if the lifetime is longer. It is also increased with increasing mobility. This effect is however offset by the diffusion length also scaling as the root of the mobility. Although the dark current scales inversely with doping the lifetime and mobility are generally reduced via impurity scattering with increasing doping complicating the picture. Also important is that the equations here are derived in the non-degenerate (dilute) doping limit. Nevertheless the scaling noted here is a useful guideline for which parameters are most important to optimize in a design.

The last term in the photovoltaic model is a second diode equation which represents the two particle recombination in the depletion region. The prefactor again contains the important physics. In the limit of only first order recombination processes being important this term is:

$$I_{o2} = qA\frac{W_D n_i}{\tau_D} \tag{4.4}$$

Here τ_D is the effective lifetime of carriers in the depletion region. Notable is that the scaling of this dark current term is again proportional to area and inversely proportional to doping (through the depletion width) and that the scaling is stronger than the quasi-neutral recombination with respect to the lifetime of the carriers.

In addition to the *pn* junction design outlined, there are also *pin* junction photovoltaics. These photovoltaics are simply the limit of an *n+/p-* or *p+/n-* junction with an additional thin heavily doped layer added on the lightly doped side of the junction. The lightly or intrinsically doped *i* layer allows for a larger depletion region while the heavily doped region allows for good contacts and a larger built in junction voltage. The advantage of a *pin* type cell over a *pn* cell is that for a fixed lifetime carriers can move farther in most cases via field transport compared with diffusive transport (the built in voltage is much larger than the thermal voltage).

As will be seen later in this chapter it is desirable to minimize the dark current in a photovoltaic. Given this reality, from the above discussion it would seem an ideal photovoltaic would be one that absorbs a large amount of light but has minimal junction area and has a very high doping but also has high carrier mobility and lifetimes. These objectives are in conflict making the design of a photovoltaic an engineering problem.

4.3 Photovoltaic performance

The objective of any solar cell is to create useable power. For a photovoltaic that power is simply the product of the current and voltage of the cell. For any physical cell there will be some maximum power point. This maximum power point is a function of how the cell is illuminated. For this reason standards have been created to allow for the comparison of one cell to another. The most commonly used illumination is air mass 1.5 (AM 1.5), which is intended to simulate the incoming solar spectrum on a sunny day at 1.5 atmospheric thicknesses (Fig-

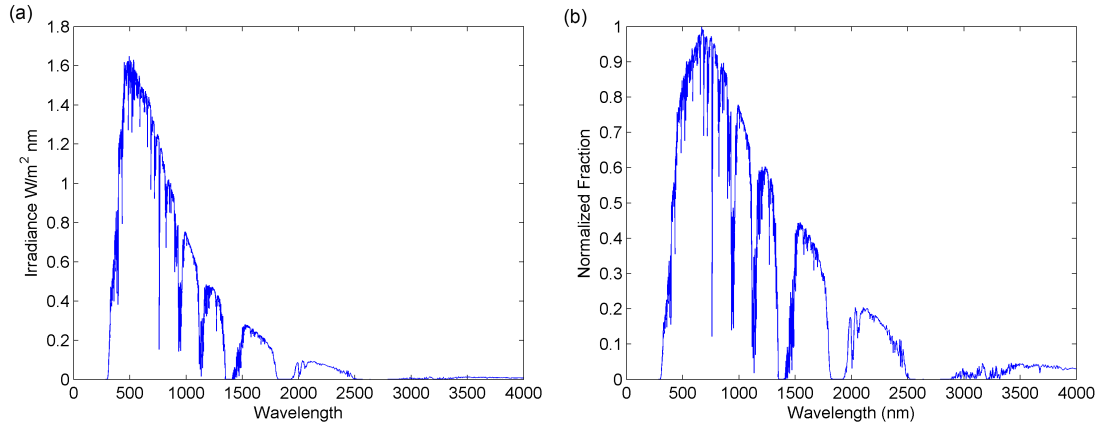

Figure 4.2: The AM 1.5 global direct spectrum is plotted as a function of power (a) and photon count (b). An ideal conventional *pn* junction photovoltaic converts all photons above its bandgap to usable current, this makes the red shifted plot in (b) more relevant than (a), however comparison shows the room for improvement possible via hot carrier photovoltaic designs.

ure 4.2). This increased thickness is used to correct for installation of solar cells at higher latitudes.

Many factors are not accounted for in a standard AM 1.5 measurement of photovoltaic performance that occur in real world application of photovoltaics. The standard measurement consists of normal incidence of the simulated spectrum onto a cell and measurement of the IV characteristics of the cell. This does not account for diffuse illumination that occurs from scattering. It also does not correctly predict properties for installations that do not track the sun where the illumination angle is not fixed at normal incidence. There are other short comings as well, but these are notable as non-planar photovoltaics will generally perform better than planar ones in both of these areas. Nevertheless a standard is needed to compare cells and later in this chapter results based on standard AM 1.5 illumination measurements are presented for VLS wire photovoltaics.

For a given illumination the amount of current collected and the operating

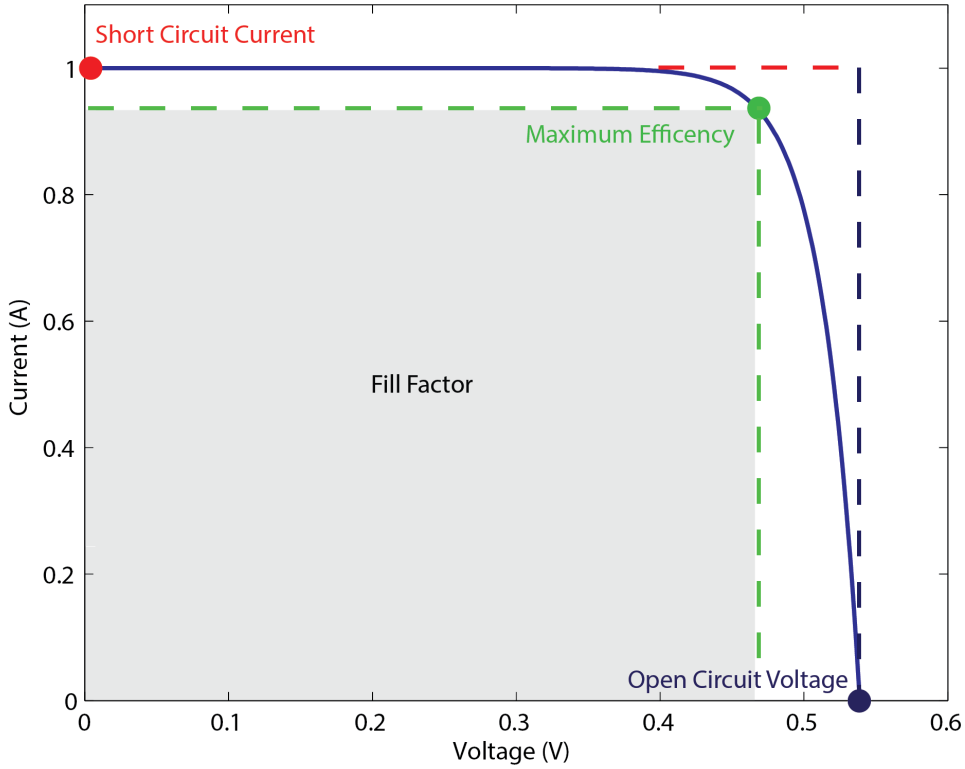

Figure 4.3: The typical figures of merit for a photovoltaic cell are illustrated in this plot. The open circuit voltage (V_{OC}) shown in blue and the short circuit current (I_{SC}) shown in red create a rectangle the area of which represents power ($P = IV$). The actual response of the photovoltaic is less than this and has a maximum power point at the tangent of the IV curve. The area this bounds is shown in grey. The ratio of the grey area to the outer bound area is called the fill factor (FF). In this simulated data the fill factor is a very large 81.2%.

voltage of the cell can be traded for one another. A typical response curve for a photovoltaic cell is plotted in Figure 4.3. The plot represents the fourth quadrant of a normal IV plot. For photovoltaics the inverted current is displayed simply to transpose the important information into the first quadrant of the plot. Figure 4.3 illustrates the common figures of merit used to characterize a photovoltaic. They are the short circuit current (I_{SC}), the open circuit (V_{OC}) and the fill factor (FF). In addition to the model of the diode action of the photovoltaic

described above, actual photovoltaics have parasitic series (R_S) and parallel (R_P) resistances, both of which degrade the cell performance. If the series resistance is much smaller than the parallel resistance (which it must be for any reasonable cell) then both the I_{SC} and V_{OC} are approximately independent of the series resistance. If the dark currents are vanishingly small and the parasitic resistances have negligible impact then the available power is the product of I_{SC} and V_{OC}. This power is represented by an area in the IV bounded by the asymptotic I_{SC} and V_{OC}. The fill factor is the ratio of this ideal power to the actual maximum power. The name fill factor comes from the idea that it is the area ratio or the amount of the ideal power area filled by the actual cell.

From the figures of merit discussed the efficiency of a photovoltaic is commonly defined as $\eta = \frac{FFV_{OC}I_{SC}}{P_{in}}$. Here P_{in} is the power available to the photovoltaic. The figures of merit parameterize the performance of the electrical side of the photovoltaic given its inherent design. Meanwhile the efficiency definition includes all ineffeciencies. It is limited to be less than the Carnot efficiency given that the cell is in thermal equilibrium. In addition to the device inefficiencies caused by non-ideal effects, a real photovoltaic based on a single *pn* junction has a single bandgap which greatly reduces the efficiency of the device; all energy of the photons absorbed above the bandgap is lost to heat. Formally these considerations are addressed in the particular case of a single junction cell in Shockley and Queisser's classic work [35]. These limitations can be removed with multi-junction cells or emerging hot carrier photovoltaics. In the case of wire photovoltaics other limitations (i.e. material properties) are more important than thermodynamic limitations. The total efficiency also includes the inefficiency of the cell at collecting photons.

As seen in the physical discussion of the *pn* junction photovoltaic, recombination is an undesirable effect. Ideally I_{SC} is equal to twice the number of photons absorbed by the cell. In reality this current is reduced via recombination. A common measure of this reduction is the so called internal quantum efficiency (IQE). This is the ratio of the electron count collected to absorbed photon count. This measure requires a parallel measure of reflectivity of a cell combined with a measure of external quantum efficiency (EQE), which is simply the ratio of the electron count collected to the incident photon count.

It is desirable to maximize each of these measures to improve photovoltaic performance. The physical reasons behind reductions in I_{SC} or IQE are clear, EHP that are created in the cell are not collected because they recombine. The physical cause of V_{OC} is somewhat less clear. Returning to the two diode model (Eq. 4.1) of the photovoltaic it is possible to invert the equation for when the current is zero. The result is more physically clear however if one of the diodes is neglected. This approximation is often true, but depends on the exact photovoltaic design. Taking the recombination in the depletion region to be zero the second diode term vanishes resulting in:

$$V_{OC} = \frac{kT}{q} \ln(\frac{I_{SC} + I_{o1}}{I_{o1}}) \approx \frac{kT}{q} \ln \frac{I_{SC}}{I_{o1}} \tag{4.5}$$

The physical cause of poor V_{OC} is also due to recombination but in a slightly more complex way. The scaling is logarithmic with recombination decreasing I_{SC} while increasing the dark current.

4.4 Design of a wire photovoltaic

The preceding discussion of photovoltaics while complex is highly simplified. It does however contain the needed results to provide intuition for design. If the design of the system was completely free this section would be extremely long, however here I restrict the discussion to wire photovoltaics both top down (made from bulk material via etching) and VLS based.

Semiconductor wires of the VLS variety seen in chapter 2 or the top down variety fundamentally are high aspect ratio structures. For simplicity here I will consider them high aspect ratio cylinders. Formation of a *pn* homojunction diode out of a Si or Ge is defined by the doping of the structure. The cylindrical geometry of a wire suggests two basic doping arrangements (Figure 4.4), a vertical junction where the doping transitions between *p* and *n* along the extruded axis of the cylinder and a radial junction where the doping transitions between *p* and *n* in the radial direction. Other doping geometries are also available but these are the simplest conceptually.

Consider first a single vertical junction wire photovoltaic. For this geometry and a fixed material (i.e. fixed bandgap, absorption, etc.) the free parameters for a design are the wire diameter, the wire height, the doping levels and their position along the extruded axis of the cylinder. Consider first the optimal diameter for this design. If the diameter is very large, and the incident light angle is parallel to the extruded axis of the cylinder then this design is simply that of a planar photovoltaic. For Si and Ge this is a very well-studied system. Choosing the doping levels and height are coupled. The height should be chosen such that it is less than the minority carrier diffusion length for a *pn* junction photo-

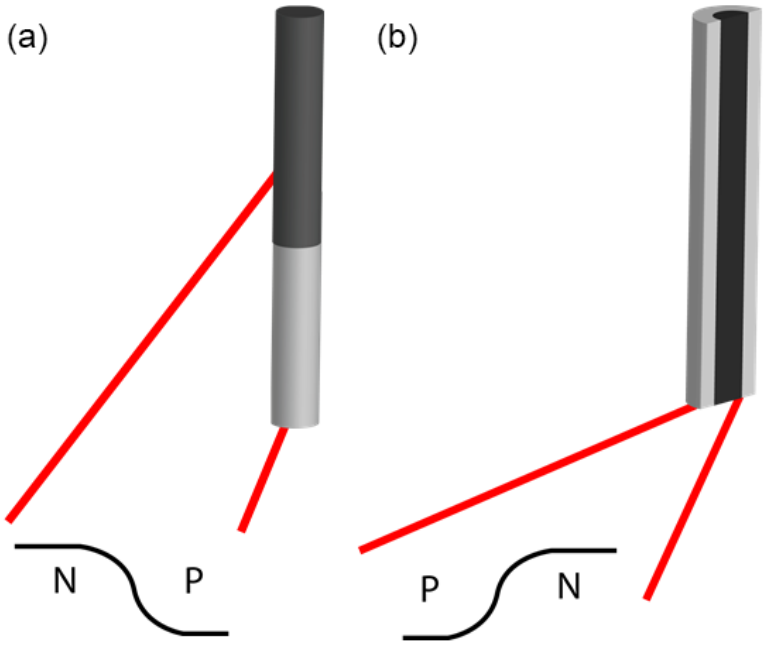

Figure 4.4: Two basic junction configurations are possible in a wire a vertical junction shown in (a) and a radial junction shown in (b).

voltaic or in the *pin* photovoltaic case so that the depletion region transit time is less than the lifetime. If the junction is placed in the middle of the wire and the height of this type of wire photovoltaic is increased then the efficiency of the photovoltaic will decrease rapidly. This is due to the masking of the useful active area with a dead area from which injected carriers cannot reach the junction. This suggests the use of a thin emitter layer at the top of the wire as is normally used in bulk planar *pn* junction photovoltaics, or limiting the total height of the wire to match the available transport length. Returning to the question of the optimal diameter this value has no apparent direct impact on the performance of this design. It does however clearly affect the number of wires needed in parallel to create a cell of a usable area. It also will affect the coupling of light into the wires via waveguide effects and the scattering of light between wires. Although there is no impact implied directly from the simple models used in

this chapter the diameter will have a strong effect on performance through the surface properties. Trapped charge at the outer interface can deplete this design radially and can also provide a large defect density in the form of dangling bonds which increase recombination. These are both negative effects which are reduced regardless of the type of surface passivation used as the wire diameter is increased. It therefore seems attractive to use large diameter wires.

The question then should be asked what if any advantage there is to small diameter wires. In terms of VLS as was seen in chapter 2 small diameter wires can be grown at lower temperatures which will can modify the material properties (lifetime, mobility, etc.) and also changes the cost of producing the material. Setting the synthesis aside and any possible material advantages related to it then there is no advantage to a small diameter wire until quantum confinement begins to modify the band structure. Wires of this diameter are difficult to mass produce and have so many surface states that it is hard to conceive of a low cost approach that would make good use of them. Therefore I will limit the discussion to wires with larger diameters where these effects are not present. For these wires decreasing the diameter simply increases the ratio of bulk vs. surface states (Figure 4.5), making the system harder to control. Therefore the largest diameter possible should be used baring desirable optical effects or material properties related to synthesis.

The major deficiency of the vertical geometry is the minimal room for improvement over the planar photovoltaic case. Wire photovoltaic's room for improvement comes from the additional geometric degrees of freedom. In the arrangement discussed above excluding scattering I have suggested the most bulk like cell possible will be the most efficient, thus they will always be worse

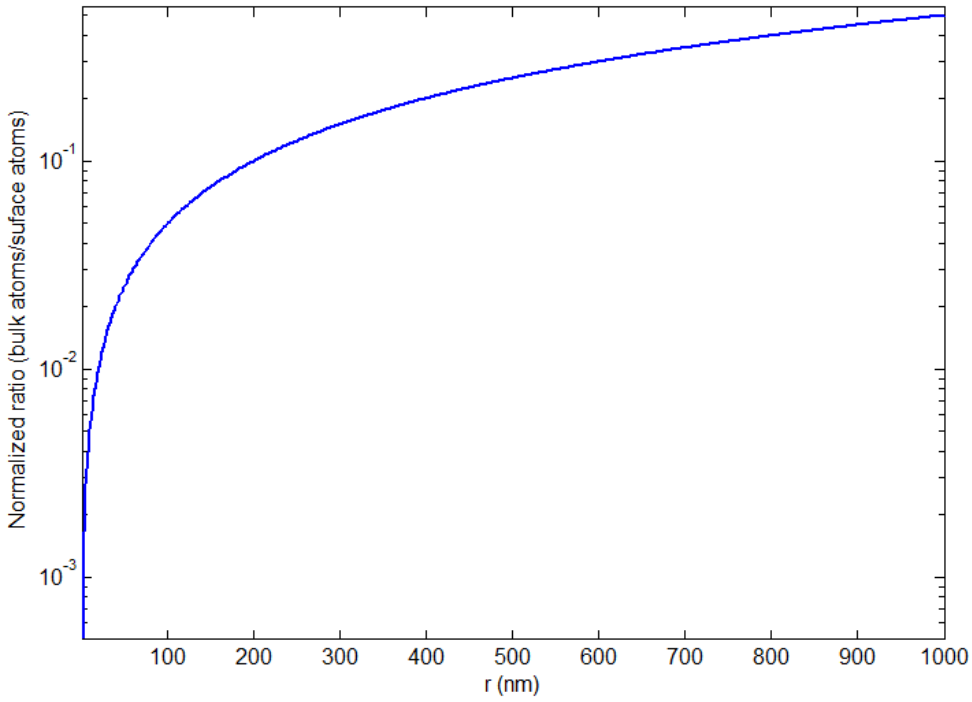

Figure 4.5: Illustrated here is the ratio of the number of surface atoms on a cylindrical Si wire to the bulk atoms. The function is normalized to a 1 micron cube of Si with a single exposed face. This was chosen as the equivalent of a "easy" to fabricate planar structure. From the plot it is clear structures under $r = 200$ nm need much more surface control. This suggests it is not worth pursuing small diameter wires unless quantum confinement effects are needed.

than a planar equivalent with equal material properties.

The major alternative to the vertical doping geometry discussed above is a radial doping geometry (Figure 4.4). In this design the light again propagates parallel to the extruded axis of the wire but the doping varies radially forming a radial *pn* junction. This makes the transport and absorption directions orthogonal to each other.

For this design it is again useful to ask what doping, diameter and height are best in the single wire case. First consider the diameter question. For this cell

design the diameter should be chosen such that it is less than the minority carrier diffusion length for a *pn* junction photovoltaic or in the *pin* photovoltaic case so that the depletion region transit time is less than the lifetime. Although the material's lifetime and mobility already suggest strongly the diameter needed for this geometry, the diameter also determines the junction area. As was seen in the model of a *pn* junction photovoltaic this area should be minimized (to minimize the dark current) which in turn implies the largest diameter possible be used. Surface state considerations also insist that the diameter be maximized. Clearly large diameter wires are desirable electrically.

Next consider the height of the wire. As the light propagates along the wire length it will be absorbed reducing the injected flux of EHP. Meanwhile the radial *pn* junction in equilibrium sets up coaxial equipotential surfaces in the wire. The injected EHP flux modifies these surfaces. Consider a thin slice of the radially doped wire as an isolated device. As the injection EHP density changes V_{OC} will change for the slice, becoming larger at high injection levels. Now consider stacking many slices on top of one another while keeping them electrically isolated from one another. In this case the slices at the bottom will have a lower EHP density and lower V_{OC} than the slices at the top. This gradient in V_{OC} creates a current when the stack is unified as a single wire with metallic boundary conditions that enforce equipotential surfaces at the terminals. This current is undesirable creating both recombination and ohmic losses and decreases the efficiency of the design. From this argument it is clear that although the light absorption direction is decoupled from the transport direction to first order this secondary effect recouples them, making a wire of great height undesirable. The exact height needed requires knowledge of the incident spectrum, intensity and absorption properties of the cell.

Finally consider the doping of this geometry. Ideally the doping should be a degenerately doped layer at the core of the wire and a degenerately doped layer at the outer shell of the wire with an annulus of lightly doped materials in between. This ideal is unfortunately not achievable in practice as will be seen.

This radial geometry seems superior to the vertical one due to the partial decoupling of light absorption from transport. It is however worth noting that the large junction area is a considerable drawback to this design as it increases recombination through interface states in proximity to the junction and the dark current though the large junction area. In spite of these reservations I pursued a radial geometry for wire photovoltaics.

4.5 Creation of wire photovoltaics

Although nano was a popular word to use at the time of this work even making its way into commercial products like the iPod nano, it is clear from the preceding discussion that nano is worse than micro in the case of photovoltaics. Essentially the ideal photovoltaic from a purely geometric and electronic point of view would be a sphere with a highly doped ball like core and a thin highly doped shell, as this would minimize the transport distances for carriers while maximizing the absorption volume. The fundamental reason nano is bad for photovoltaics, excluding quantum effects, is that photovoltaics are volumetric devices and decreasing the size simply increases the surface area which is bad in terms of control and dark current.

From this argument it is clear why I pursued growing relatively large VLS wires rather than small nanowires. The method of growing large VLS wires

was covered in chapter 2. For the purposes of creating photovoltaic devices top down wires were also employed. These wires were created from single crystal wafers via Cl RIE and conventional photolithography. A thermal oxide mask was used for the Cl etching. This mask was defined by transferring the resist pattern into the oxide using a CHF_3/O_2 RIE. The purpose of creating top down wires was to have control samples for the cell geometry and photovoltaic fabrication process excluding wire formation/materials.

VLS wires can be grown epitaxially on a single crystal substrate or non-epitaxially on an amorphous substrate. As seen in the chapter 3 on an amorphous substrate the wires have no preferred orientation relative to the substrate but remain single crystals. To compare VLS wires to top down wires and match their geometry, epitaxial VLS wires were employed. The height chosen for the initial work was somewhat arbitrary at nominally 8 μm. This height was selected because the available Cl RIE tool was able to etch to roughly this depth while maintaining reasonably vertical sidewalls. The spectral efficiency for a single absorption pass as a function of length in Si is plotted in Figure 4.6.

Both the epitaxial VLS wires and top down wires used to create test photovoltaics were patterned in a square array for simplicity. From a scattering perspective this is clearly not ideal as such an array represents a photonic crystal with photonic bandgaps. Studies have been done to assess the efficiency of different arrangements of wire photovoltaics optically [36], showing that complex tiling or random arrangements perform best. Here however the goal was simply to compare VLS materials to top down materials for photovoltaic applications.

To create the desired radial *pn* junctions the Si must be doped in a control-

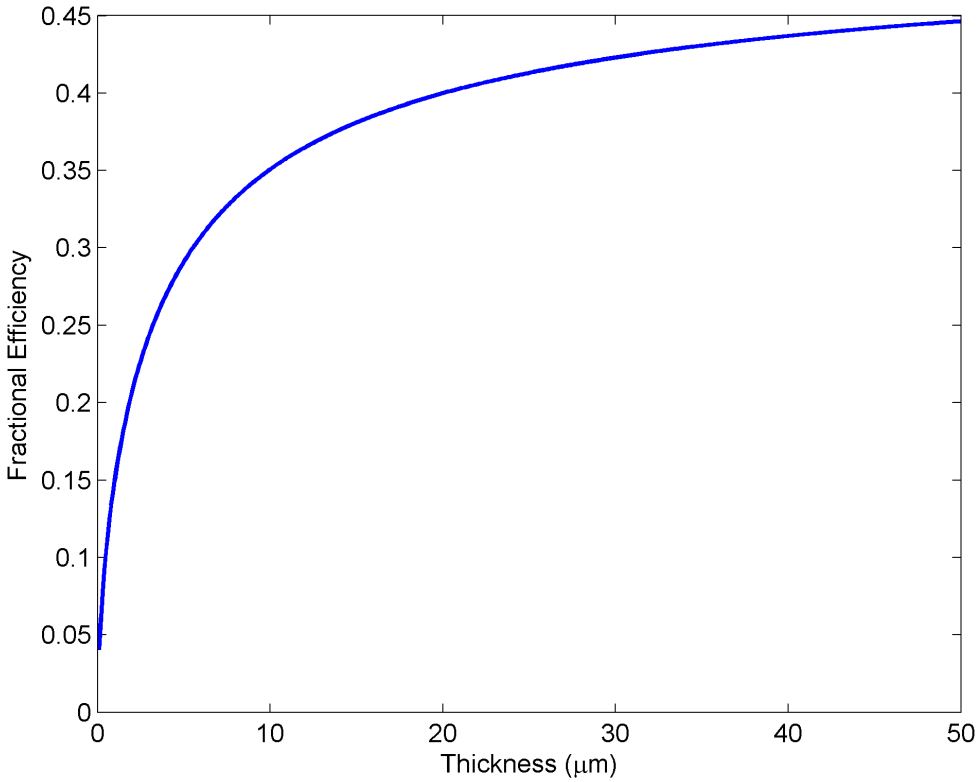

Figure 4.6: This figure shows the maximum possible efficiency of a single absorption pass bulk band structure Si photovoltaic as a function of thickness for an global direct AM 1.5 spectrum (excluding black body effects for simplicity).

lable manner. This is actually somewhat difficult, particularly in the VLS case. Although not covered in chapter 2 it is possible to create doped material directly during the VLS process simply by adding doping precursors to the reactor in similar fashion to conventional CVD growth. This seems superficially simple but in actuality it is not. The reason is that the phase diagram and bonding energies for the dopant are not the same as that of the crystal being precipitated out, this means a very different rate of absorption and precipitation occurs for the two different types of atoms. In addition recall that in VLS for large Si wires there is a background CVD rate. This material grows without the use of the catalyst and thus would have a different doping density than the VLS material for

any gas mixture. This variance might be exploitable in some cases but for the present case I chose simply to grow nominally undoped VLS materials and dope them after synthesis. I use the word nominally with care here, both because the CVD reactor will have a background impurity level which is unavoidable and also because the wafer on which the epitaxial VLS wires are grown is a source of doping.

This second source of doping is worthy of further consideration. Clearly if a VLS wire is grown on a doped substrate there will be diffusion from that substrate at the elevated temperatures of VLS growth. However the textbook diffusivities in Si of common dopants (P, B, As) at the synthesis temperatures used (600-750 C) are so low such diffusion is completely negligible in the synthesis time. However these diffusivities are valid only for a bulk crystal. The large surface area or other VLS material properties may greatly increase these diffusivities; they therefore represent a lower bound. In addition to normal diffusion the epitaxial VLS process absorbs some of the substrate in the eutectic particle. Thus the melt from which the VLS wire is grown initially should have a doping that matches the substrate. This precludes an abrupt junction at the wire/substrate interface. The most reasonable model for the relaxation of this doping is exponential. This assumption may be modified by free energy effects at the liquid-solid interface however that impede or enhance the precipitation of the dopant. Assuming an exponential relaxation and an initial Si concentration of 20% entirely from the substrate in the catalyst, this implies a doping relaxation of 3 orders of magnitude in about 1.38 diameters.

The ideal doping profile of a radial *pn* or *pin* diode is a heavily doped inner cylinder, a lightly doped annulus and a heavily doped shell. This configuration

minimizes the core resistance of the wire reducing parasitic series resistance in the cell while allowing the depletion layer thickness to be maximized. Unfortunately this is not possible to physically construct. No matter what method is used the doping of a wire is either uniform or greater at the outer surface. This is because the dopants enter from the outer surface of the wire inward. This means the center of the wire is at best uniformly doped. Doping the wire via diffusion from the substrate, $POCl_3$, solid phase diffusion from doped glasses and ion implantation were all used at different times to construct photovoltaics. For top down wires the wafer's doping was used for the uniform core doping. For VLS wires after ion implantation or other doping means, long thermal annealing (up to 12 hours) in N_2 was used to make the doping uniform.

Following this anneal step, highly doped polysilicon of the opposite type was deposited on the wires forming a radial *pn* junction. However this junction's depletion region is at a very dirty polysilicon/single crystal interface. This interface contains many dangling bonds and other defects that are active recombination centers. Therefore the cells were annealed to drive the junction into the single crystal core of the wire. This anneal amount was varied to empirically determine the best time typically on multiple cells being processed in parallel. IVs were taken under an uncalibrated light microscope for each test anneal. Annealing too short a time leaves the depletion region interacting with the dirty polysilicon interface. Annealing too long pushes the junction into the substrate as the heavily doped polysilicon layer has many orders of magnitude more dopants than the other active layers. The optimal anneal is between these. A typical time and temperature for this anneal step would be 900 C in N_2 for 30 minutes for *p*+ polysilicon doped with B.

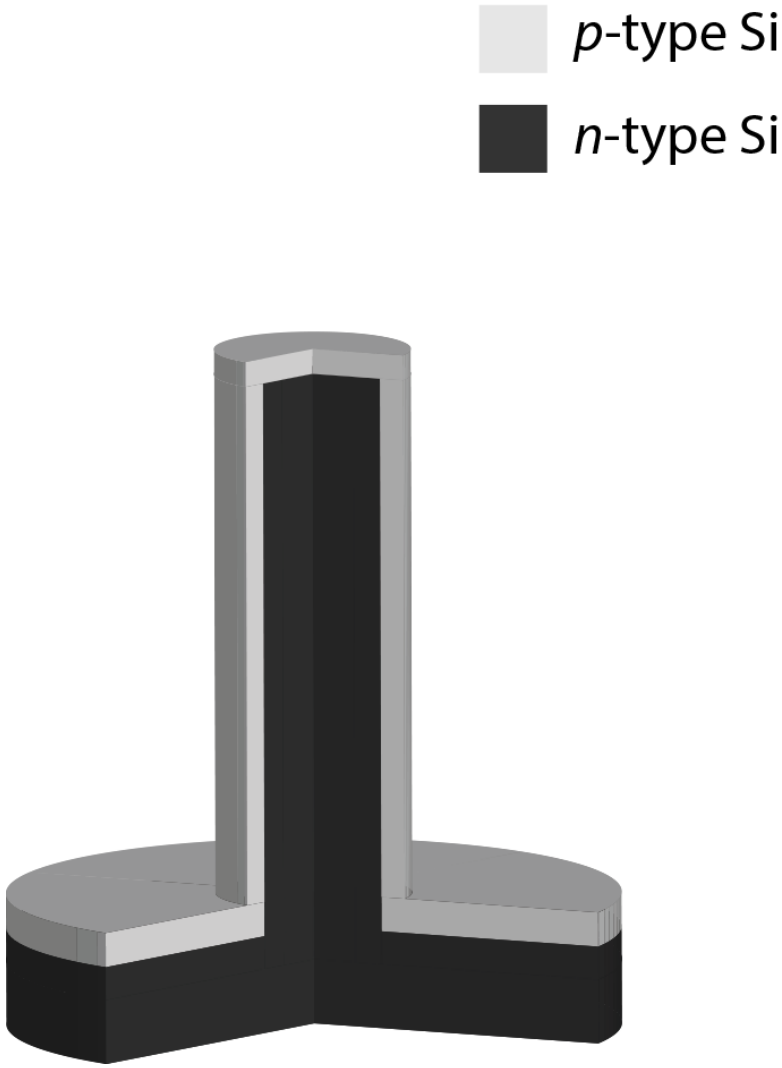

Figure 4.7: This diagram shows the simplest configuration of a wire *pn* junction. The conformal *p* layer forms a junction both with the VLS wire material but also the substrate. This system is best thought of as two different types of diodes in parallel each with its own photo response.

The cell construction as described above is shown in Figure 4.7. It consists of a support substrate, uniform core of the same type, and a polysilicon contact layer of the opposite type used to counter dope an annulus in the VLS or top down material. The polysilicon CVD step also has the virtue of providing a conformal contact to all wires regardless of orientation or shadowing effects. Metallic contacts were made to the cells on the front and backsides of the sub-

strate, the front side contact connecting to the polysilicon layer and the backside contact connecting to the wire core via the substrate. These contacts were annealed at 350 C in N_2 to improve contact resistance. Ti was used for *n*-type contacts and Pt was used for *p*-type contacts. All contacts were made via liftoff in an electron beam evaporator at a pressure no more than 2 μTorr following an HF dip to remove native oxide.

The cell construction shown in Figure 4.7 will result in the best possible efficiency for this scheme of doping geometry. However, as drawn it contains a large parallel polysilicon substrate junction. While this diode may be efficient is not the main object of study. Therefore additional steps are needed to isolate this junction from any measured results. One means to removing this junction is to place a thin oxide layer between the polysilicon and the substrate, as shown in Figure 4.8.

The reader may have wondered why polysilicon was used to provide the counter doping needed to form the coaxial wires given the possible introduction of defects near the junction with such a process and the impossibility of those defects if some other source of doping was used. The reason is made clear by Figure 4.8. In this configuration each diode's outer layer is isolated at the substrate; some contact must be used and while a layer of metal or transparent conductor such as ITO is conceivable polysilicon is much safer. Metals can short a junction exposed by breakage between the counter doping and contact steps. Polysilicon by virtue of being both steps combined removes this hazard.

There remains a problem with the design in Figure 4.8 for studying the efficiency of VLS photovoltaics. Although the substrate is now isolated in that no diode is formed with the polysilicon layer, the substrate can still serve as an

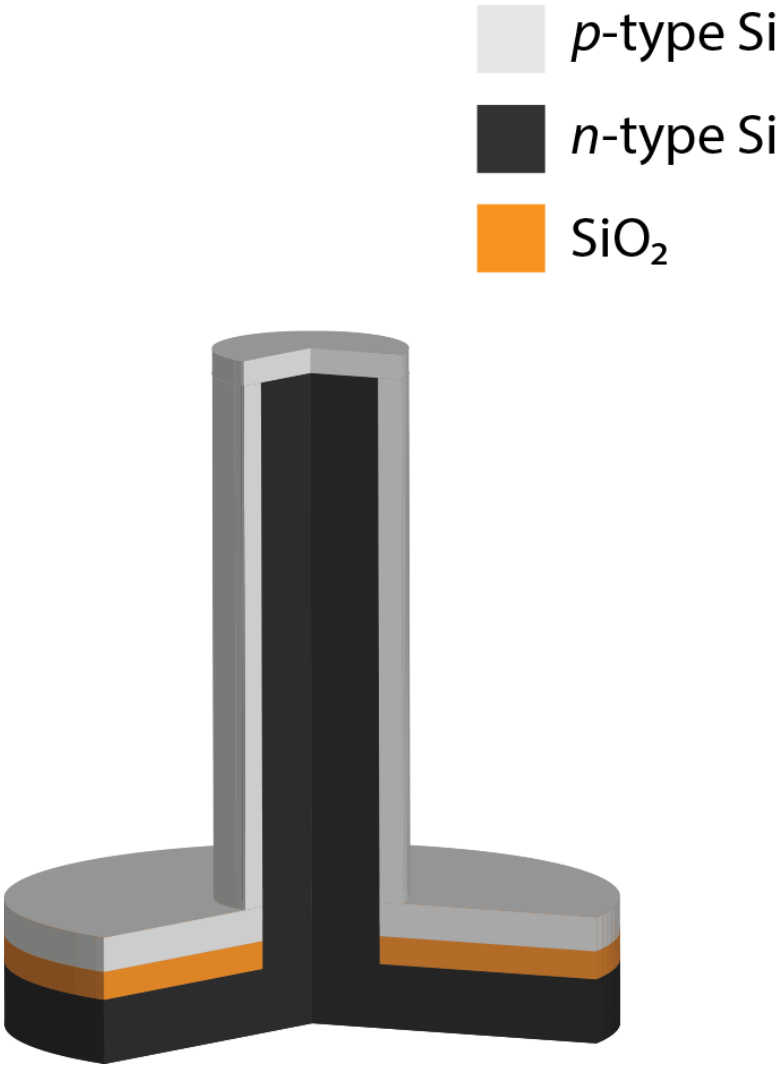

Figure 4.8: This diagram adds an isolation oxide to the the simplest configuration of a wire *pn* junction. This oxide layer separates the conformal *p* layer from the substrate forcing it to only form a junction with the VLS material. In this configuration carriers can still diffuse from the substrate creating photocurrent.

injection source of electrons or holes. It is quite likely to have a much longer lifetime than the wire materials. This means carriers created in the substrate can diffuse to the wire and become a major contributor to the efficiency of the cell.

There are two possible means to get around this issue. One is to dope the substrate heavily enough that its lifetime is reduced and the contribution be-

comes small. Another is to provide a blocking layer of wire material. In truth modification of the doping profile of the substrate is not enough no matter what it is set to as the properties of the wires are totally unknown. Nevertheless some studies rely on doping alone to block carrier injection [37]. I chose to use the wire material to block injection. This simply requires moving the oxide layer that isolates the substrate up the wire sidewall. Any carriers created in the substrate must then pass through this extra wire material effectively blocking injection from the substrate. With this arrangement the studied cell is then of shorter height than the wire height but the results are clearly from the wire materials. Such a cell is shown in Figure 4.9.

To accomplish the configurations shown in Figures 4.8 and 4.9 the wires were first thermally oxidized to form a conformal insulator. Next the wires were carefully coated with resist via standard spin coating. This resist was etched in a RIE with O_2 to expose the tip of the wires. The cells were then dipped in buffered HF and the HF allowed to wick down the sidewalls of the wires. By adjusting the time of this last step the height of the oxide layer on the wire sidewall can be changed.

Initially *n*++ <111> wafers doped with As were used to create the VLS wire photovoltaics and cells with a minimal thickness blocking layer used. Heavily doped wafers were chosen to simplify contacting the substrate. These wafers often produced results in photovoltaics with ohmic IV response. The minimal blocking layer thickness combined with the doping effects already noted likely formed tunnel junctions at the base of the wire resulting in this observation. Addition of the thicker blocking layer removed this issue creating separation between the highly doped *n* and *p* materials. Lightly doped *n* (phosphorus) and

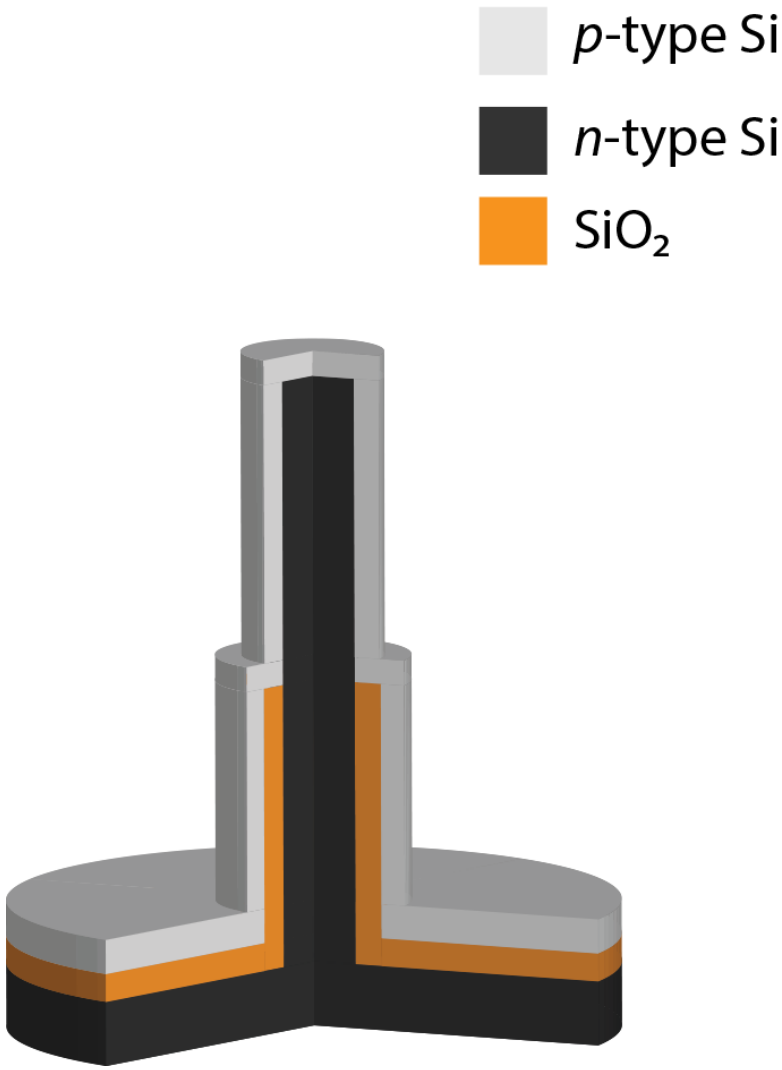

Figure 4.9: By extending the oxide isolation layer up the sidewall of the wire this configuration offers a thickness of VLS material at the base of the wire that blocks carrier injection from the substrate. This allows the properties of the VLS junction to be observed without complicating injection effects.

p (boron) substrates were also used. These required an extra implantation on the backside of the wafer to allow for good ohmic contact but otherwise had no IV related complications.

Initial photovoltaics were made as 100 × 100 μm squares however this size was too small for the solar simulator setup to measure accurately. After initial

Sample	Eff. (%)	I_{SC} (mA/cm^2)	V_{OC} (V)	FF (%)	R_S (Ω)	R_P (kΩ)
VLS Cell 1	0.68	4.27	0.324	49.1	60	59.7
VLS Cell 2	0.64	4.28	0.315	47.6	60	59.7
Etched Cell 1	5.15	18.65	0.469	58.8	66	514
Etched Cell 2	5.12	18.30	0.471	59.2	81	750

Table 4.1: Typical results for top down (etched) and bottom up (VLS) wire photovoltaic cells under AM 1.5 illumination.

measurements a cell size of 2.5 × 2.5 mm was selected with 2 μm pitch square array of wires. The resulting cells contain 1.5625 million diodes in parallel. This is an active device count around that of a 486 processor. It is a very challenging amount of devices to have work without major defects. A 2.5 × 2.5 mm cell size was as small as was reasonable for the solar simulator. Normal test photovoltaics are at least 1 square cm. It is worth considering that this count is for a photovoltaic with large wires. A small wire photovoltaic would have even more devices in parallel. A typical complete cell is shown in Figure 4.10.

4.6 Wire photovoltaic results

Wire photovoltaics based on top down etch wires and VLS wires grown from Au were created using identical processing save for the etching and wire synthesis steps that inherently must be different. These cells were measured in an AM 1.5 solar simulator at IBM Research. Typical results for test cells can be seen in Figure 4.11 and Table 4.1.

Several things are clear from the results immediately. The top down photovoltaics are significantly better than the VLS based ones. They have similar series resistance but the VLS cells have lower parallel resistance, higher dark current, lower short circuit current, and lower open circuit voltage. Addition-

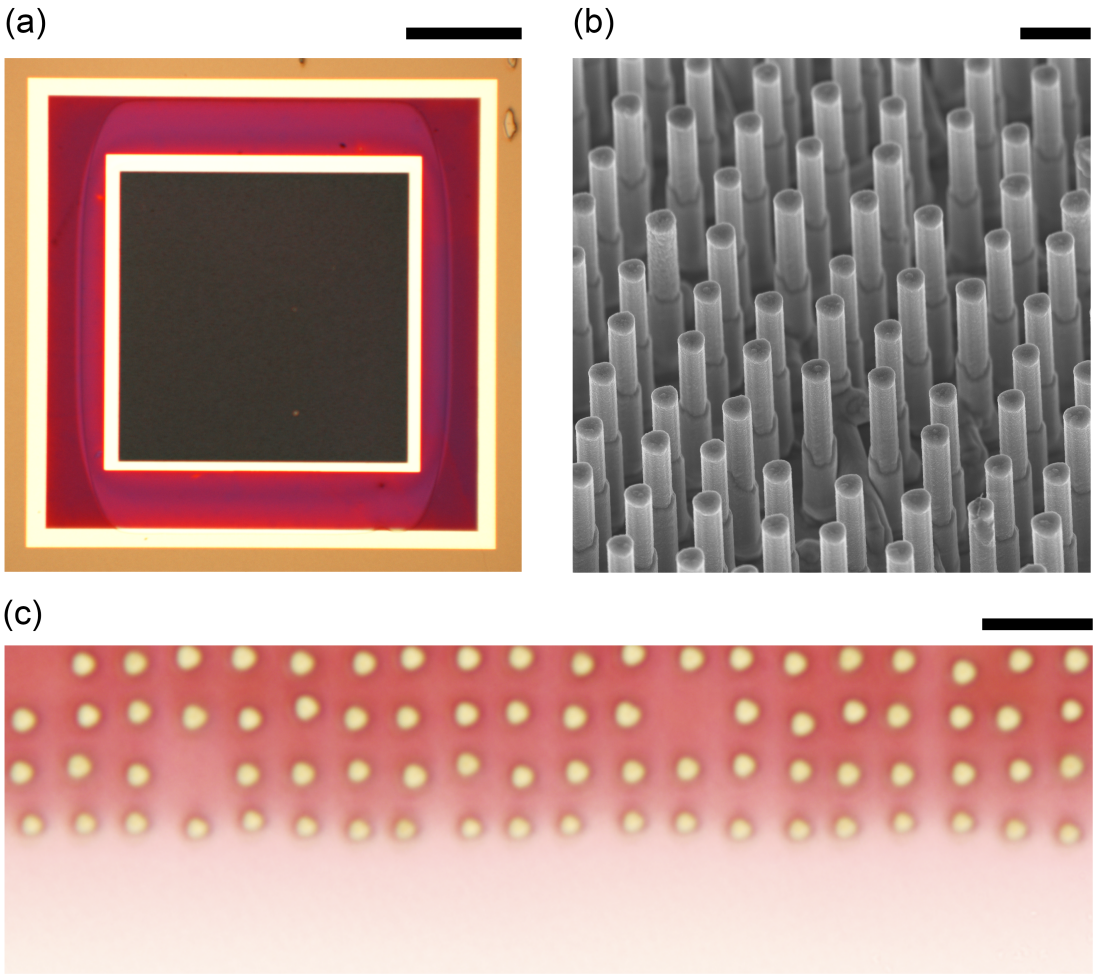

Figure 4.10: (a) Shown is a complete 2.5 × 2.5 mm VLS wire photovoltatic. The layers from the outside inward are the substrate, the polysilicon clading, and annealed metal contact layer, polysilicon clading and finally the wire array. (b) An SEM of the same photovoltatic shows the implementation of the structure in Figure 4.9. The discontinuity on the sidewall is the position of the oxide layer. (c) At high magnifications optically the wire array is red shifted as more of these longer wavelengths are able to reach the bottom of the array and return without being absorbed. This image is at the edge of the array. The scale bars are 1 mm, 2 μm, and 4 μm for (a), (b) and (c) respectively.

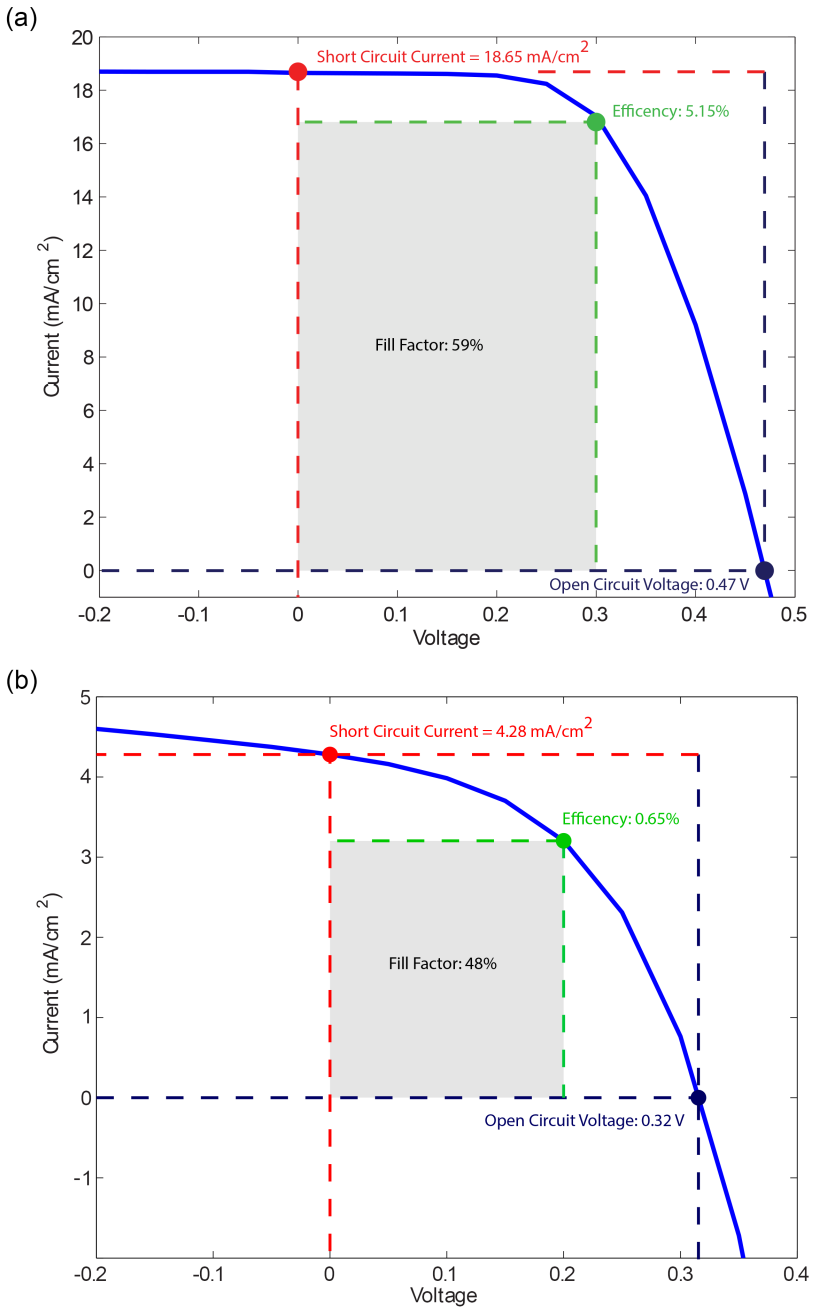

Figure 4.11: Results for top down (a) and VLS (b) wire *pn* junction photovoltaics under global direct AM 1.5 illumination are shown. Although the geometry and fabrication process excluding wire formation are similar the top down etched wire photovoltaic is significantly better than the VLS photovoltaic. The top down design suffers from a low open circuit voltage relative to its short circuit current (the FF is not square), suggesting it is suffering from a mismatch between the large junction area and the available diffusion length. The VLS is better matched but has worse properties overall.

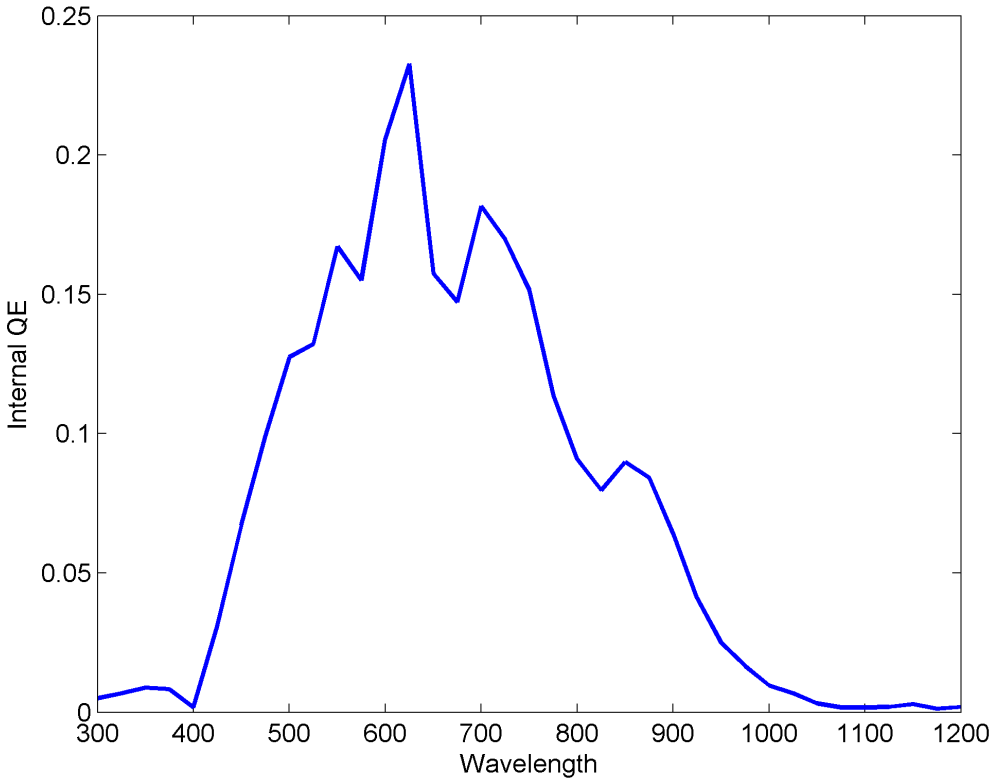

Figure 4.12: Shown is the IQE of a typical VLS photovoltaic analogous to those reported in Table 4.1. It clearly shows that across wavelengths recombination is preventing carriers that are injected from being collected.

ally with this design the measured ideality factor of the exponential region in dark IVs was near 2 for VLS materials and near 1 for the top down materials. This suggests significant recombination in the depletion region in the VLS cells. Measurements of IQE confirm this (Figure 4.12). The high ideality factor and poor IQE suggest a better doping profile for the VLS cell would result in better performance. Such a profile requires a larger doping gradient which was difficult to achieve in practice without even greater shunting losses.

Given that all possible steps in the process flow were made identical these observations strongly point to the VLS material being inferior to the top down

material. The observed performance difference directly caused the investigation into the lifetimes of VLS materials that is the subject of chapter 5.

The VLS cells show significantly worse shunting than the top down cells, with an order of magnitude worse parallel leakage. This leakage current can be from many sources including tunnel junctions, direct shorts, and recombination current. Inherently the VLS photovoltaic cells are more defective than the top down equivalent as not all of the wires are vertical. In VLS cells the diameter of the wires varies due to catalyst volume effects caused by both migration and deposition variance. Additionally the defects present in each wire conceivably vary more in VLS cells, than in top down cells.

To see impact of defective wires on this type of photovoltaic consider a single wire with cross sectional area of 1 μm^2 and length of 10 μm doped to 1×10^{16} per cubic cm with phosphorus. At this doping level the resistivity of the wire is nominally 0.5 ohm-cm. This means a single completely shunted wire would provide a 50000 ohm leakage path. Although this number is comparable to the parallel leakage observed in the VLS cells the leakage is not observed to vary in integer steps suggesting this is not the type of defect that dominates the parallel leakage in VLS photovoltaics. It does however show how difficult an effective wire photovoltaic is to make. Single site defects can completely destroy the cell performance, given the vast number of devices in parallel and the fragility of the devices this is a major practical hurdle for wire photovoltaics, particularly given the need to reduce the series resistance of the photovoltaic to a minimum which likely requires a transparent metal contact such as ITO. Such a layer would create a short across any junction exposed due to mechanical breakage of a wire. The exclusion of direct shunting of the wires as a likely cause

of the lower parallel resistance in the VLS cells reinforces the need to study VLS material properties such as lifetime to understand possible defects that might create leakage through the junction itself.

Given the possible variation between wires in the VLS cells it is also prudent to observe individual wire contributions to the overall photovoltaic. To do this a scanning photoconductance setup in Prof. Paul McEuen's lab was used with the help of fellow graduate student Arthur Barnard. For this work a tunable Ar Ion CW laser was employed. The laser power was set to 50 μW chopped with a spinning disc and focused onto the sample using an inverted optical microscope. The scanning was provided via two galvo mirrors. Readout of the photocurrent was provided via a lock-in amplifier locked to the chopper frequency. Use of a lock-in removed DC photocurrent contributions from room and other stray lighting while providing the sensitivity to measure individual wire contributions easily.

For this measurement a new design of photovoltaic was made (Figure 4.13) similar to the *pn* junction photovoltaic with the background layer shown in Figure 4.7 but including an Al mirror layer to prevent light from entering the photovoltaic anywhere but the tip of the wires. This work was completed after the lifetime work discussed in chapter 5. In addition to wire variations I had hoped it would be possible with this experiment to observe changes in efficiency as a function of wavelength allowing further knowledge of transport in the photovoltaic. This is in principle possible as the absorption length of different wavelengths changes the injection distribution provided in each wire. In practice this proved problematic due to difficulties in focusing the laser on the tips of the wires reproducibly across wavelengths. In short because the focus

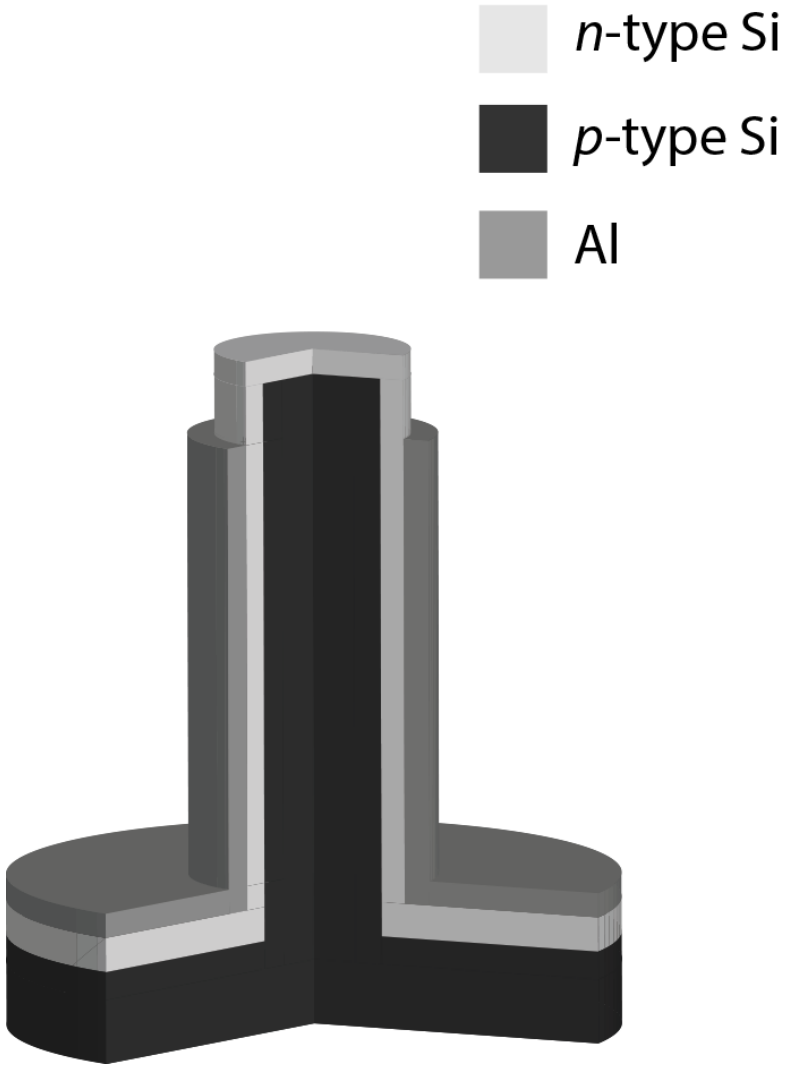

Figure 4.13: Although the blocking scheme used largely prevents injected photocurrent from the substrate, an alternative Al mirror layer is shown here to accomplish the same task. This structure has lower contact resistance but a higher risk of shorts. It was constructed to allow the light to enter only at the tip of the wire, and thus in principle allow the probing of the transport and recombination as a function of depth by varying the wavelength and thus the absorption length. In practice this proved difficult systematically to measure, the device concept shown here however is sound.

shifts and diffraction limit changes as a function of wavelength there is no simple means to know that the same number of photons are being injected across wavelengths, making a spectroscopic measurement difficult. Time constraints and other projects precluded full exploration of this technique however the initial data does show wire to wire variations in photocurrent (Figure 4.14). SEM observations of the area probed show no observable differences wire to wire save for diameter variations (Figure 4.15). However optical variations are easily notable (Figure 4.16) particularly when focused on the very top of the wires (as was the case in the photoconductance measurement), therefore the observed photocurrent variations are likely largely an optical effect rather than a transport one. As discussed a single truly defective wire will greatly impact the overall cell. Instead the more likely cause for the poor performance of these VLS photovoltaics is the VLS materials and the non-optimal doping geometry.

4.7 Summary

Creation of highly efficient photovoltaics based on VLS materials is challenging. Such photovoltaics integrate large numbers of active devices in parallel and require defective device rates significantly better than 1 in a million. While achievable such low defect rates add to cost. Cost combined with efficiency is paramount in photovoltaics. The Si VLS materials grown via SiH_4 in this chapter are not promising for commercial applications. Other VLS reactions may provide better materials, however yield, fragility, and large junction areas remain weaknesses of wire photovoltaics. They do however give significant scope via their geometric degrees of freedom to optimize both transport and optical properties. In spite of these freedoms solar cells remain volumetric de-

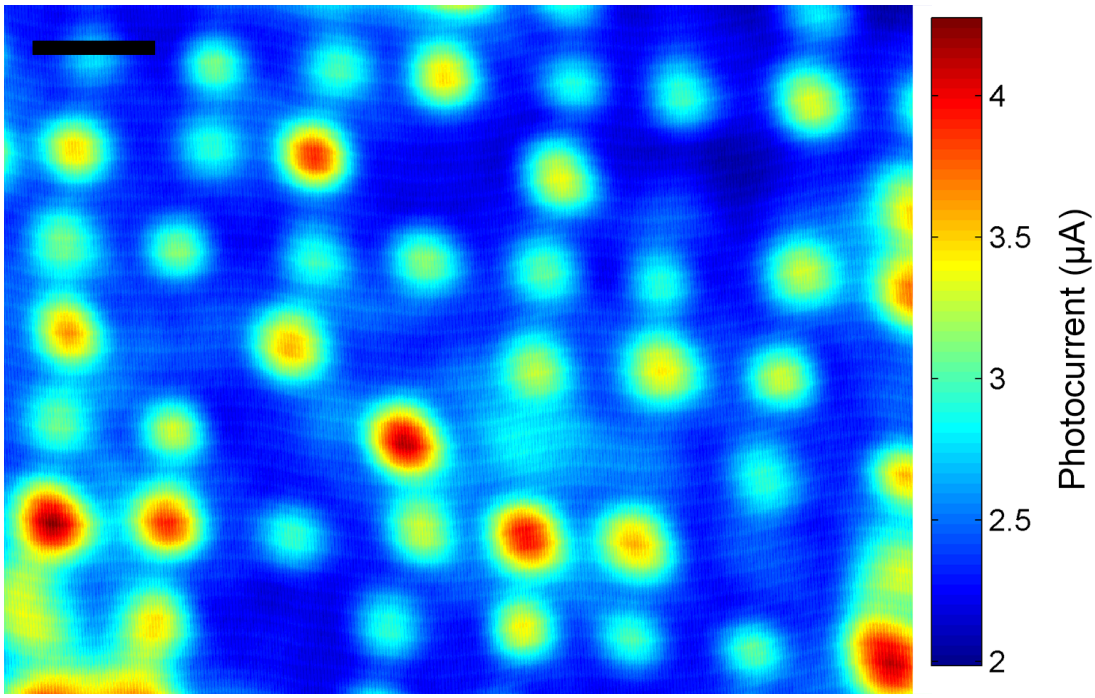

Figure 4.14: A scanned photoconductance image of the wire photovoltaic shown in Figures 4.15 and 4.16. The laser light was focused on the tips of the wires and was sourced from an Ar ion laser set at 488 nm for this image. The beam was attenuated to a power of 50 μW and chopped at 5 KHz. This reference frequency was fed to a lock-in amplifier to take the image seen. The fine features in the image are due to scanning and chopping related artifacts. There are significant variations in the photocurrent, but the majority of wires are similar with a few outstanding wires rather than a few bad wires. The scale bar is 2 μm.

vices favoring materials which have low surface to volume ratios, or extremely well controlled surfaces, factors which favor more traditional thin film type approaches.

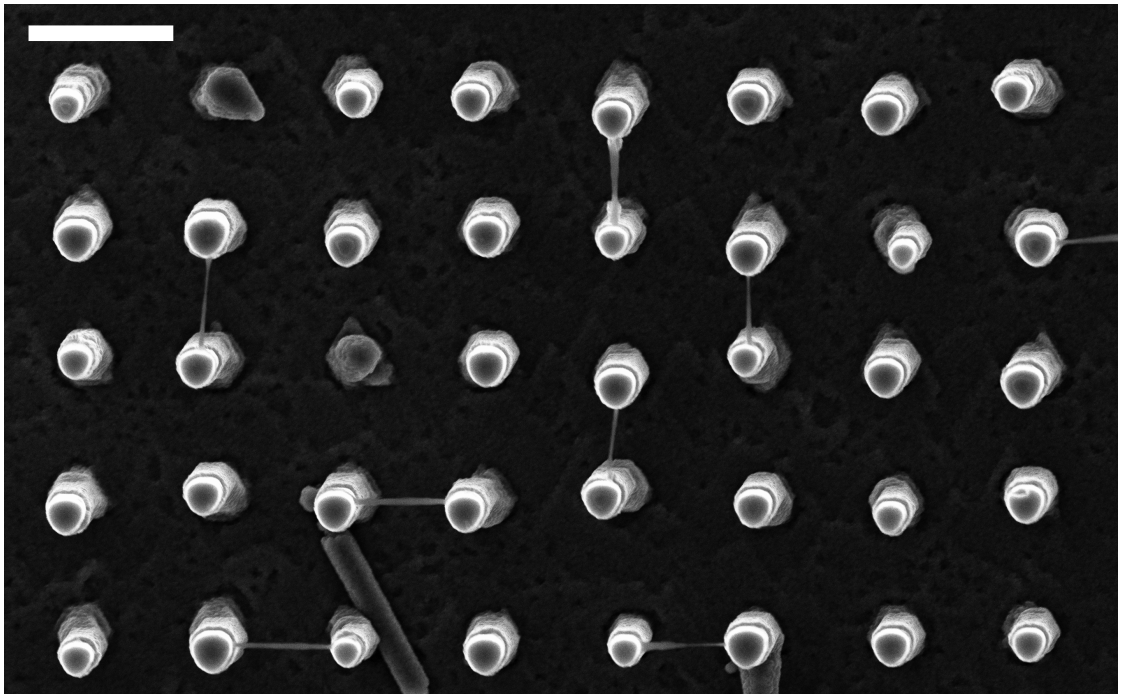

Figure 4.15: There is little difference observable wire to wire in SEM observations of the arrays measured via scanned photoconductance. The material bridging the wires is Al deposited on what was likely a thin resist filament remaining behind between processing steps. This view shows the exposed tops of the wire photovoltaic and the Al mirror cladding. The scale bar is 2 μm.

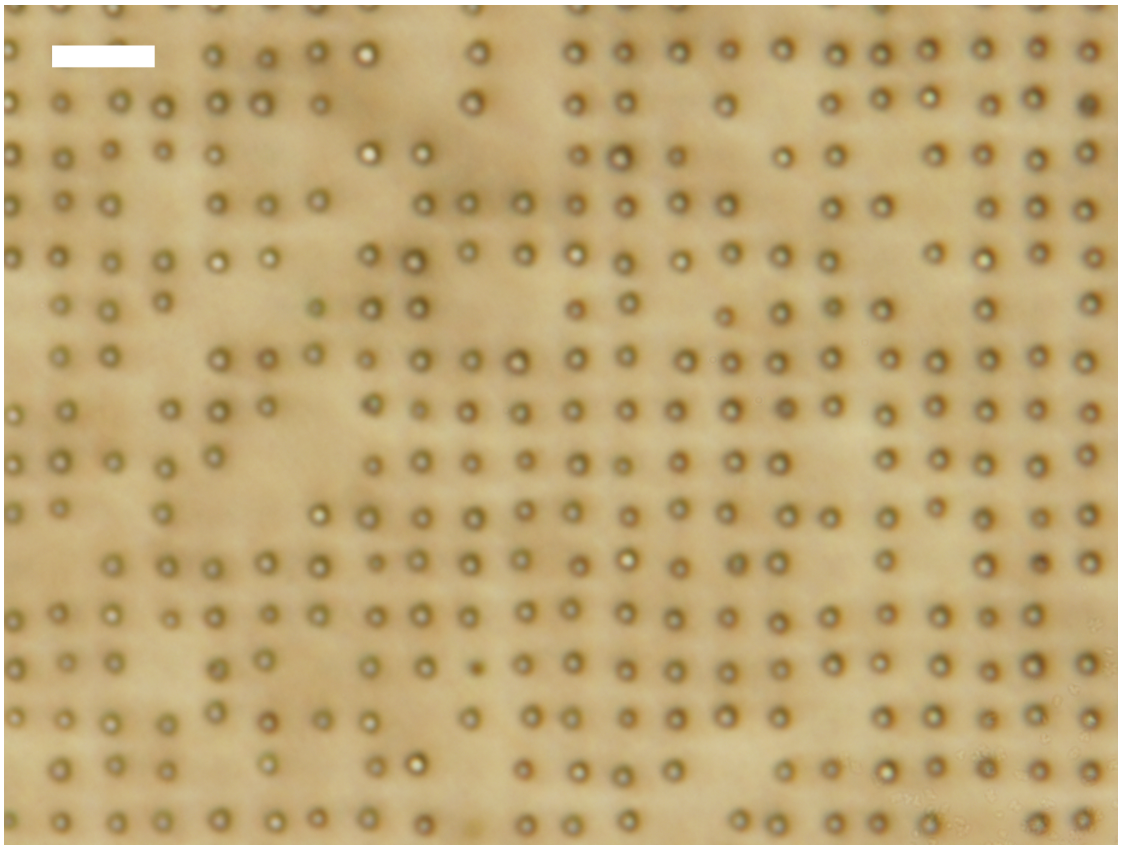

Figure 4.16: This optical micrograph is focused on the tips of the wires, it shows several wires in the array that have a different contrast around them then the remainder of the wires. This contrast difference is likely the source of the difference in photocurrent observed in the scanned photoconductance. The scale bar is 4 μm.

CHAPTER 5

CARRIER LIFETIMES OF SILICON VAPOR-LIQUID-SOLID WIRES

5.1 Introduction

Semiconductor devices rely critically on material purity for their properties. The basis for nearly all semiconductor devices is the introduction of a relatively small amount of intentional impurities (dopants) that create electronic states inside the bandgap. Unwanted states are defects, some of these are benign and some interfere with a desired behavior of the device.

As was seen in chapter 4 photovoltaics made of Si VLS materials are significantly outperformed by top down wire photovoltaics. This performance difference suggests defects that are not benign in the VLS grown materials. VLS materials potentially suffer from a large number of surface states due to their high surface area as well as metal incorporation in the lattice from the catalyst. Both introduce defect states that cause trap-mediated non-radiative recombination, which reduces carrier lifetimes. This makes measurements of lifetime a sensitive measure of material quality.

To assess material quality as the potential cause for the performance gap between the top down and bottom up (VLS) materials, experiments to measure the carrier lifetimes of VLS materials were undertaken. These investigations are the subject of this chapter.

5.2 Recombination in vapor-liquid-solid semiconductor wires

Before discussing the design, simulation and experiments of this investigation it is worthwhile to briefly review the basic recombination mechanisms for carrier concentrations out of equilibrium. There are three major classes of recombination in semiconductors: direct band-to-band recombination, Auger recombination, and defect mediated or Hall-Shockley-Read (HSR) recombination.

An excellent review of this topic in the context of Si written by Schroder [38] is well worth reading in full, as is the chapter on carrier lifetimes in his book on semiconductor characterization [39]. The most important results of this topic are repeated here for completeness.

Recombination processes occur in parallel therefore their rates simply add. Given that the lifetime is the inverse of the rate the lifetimes add inversely:

$$\tau_{total} = \frac{1}{\tau_{HSR}^{-1} + \tau_{Rad}^{-1} + \tau_{Auger}^{-1}} \tag{5.1}$$

HSR recombination is mediated through deep-level defects inside the semiconductor gap. In this case the lifetime is given by HSR theory [40]:

$$\tau_{HSR} = \frac{\tau_p(n_0 + n_1 + \Delta n) + \tau_n(p_0 + p_1 + \Delta p)}{p_0 + n_0 + \Delta n} \tag{5.2}$$

With the following definitions:

$$n_1 = n_i e^{(E_T - E_i)/kT} \tag{5.3}$$

$$p_1 = n_i e^{-(E_T - E_i)/kT} \tag{5.4}$$

$$\tau_p = \frac{1}{\sigma_p v_{th} N_t} \tag{5.5}$$

$$\tau_n = \frac{1}{\sigma_n v_{th} N_t} \tag{5.6}$$

Here E_i is the intrinsic Fermi level of the semiconductor, E_T is the energy of the trap level, n_i is the intrinsic carrier density of the semiconductor, v_{th} is the thermal velocity, σ_p, σ_n are the conductivity of the holes and electrons respectively, and $\Delta n, \Delta p$ are the excess numbers of hole and electrons respectively.

It is worth considering the HSR mechanism in two limits one a perturbative or low injection level limit and the other in the limit of high injection. In the high injection level limit this expression reduces to:

$$\tau_{HSR} \approx \tau_p + \tau_n \tag{5.7}$$

In the low injection limit the expression reduces to:

$$\tau_{HSR} \approx \frac{n_1}{p_0}\tau_p + (1 + \frac{p_1}{p_0})\tau_n \approx \tau_n \tag{5.8}$$

Radiative recombination is the next term to consider. The functional form of this recombination is:

$$\tau_{Rad} = \frac{1}{B(p_0 + n_0 + \Delta n)} \tag{5.9}$$

In the high injection level limit this expression reduces to:

$$\tau_{Rad} \approx \frac{1}{B\Delta n} \tag{5.10}$$

In the low injection limit the expression reduces to:

$$\tau_{Rad} \approx \frac{1}{Bp_0} \tag{5.11}$$

Following Schroder [38] it is worthwhile to lump radiative/direct band-to-band recombination together with trap assisted Auger recombination. Direct recombination is small in Si due to its indirect bandgap with a typical value of

$B_{Rad} = 2 \times 10^{-15}$ cm^3/s. The magnitude of trap assisted Auger processes is similar ranging from 1×10^{-15} to 9×10^{-15} cm^3/s in bulk silicon.

The last term to consider is regular Auger recombination. The functional form of this recombination is:

$$\tau_{Auger} = \frac{1}{C_p(p_0^2 + 2p_0\Delta n + \Delta n^2) + C_n(n_0^2 + 2n_0\Delta n + \Delta n^2)} \tag{5.12}$$

In the high injection level limit this expression reduces to:

$$\tau_{Auger} \approx \frac{1}{(C_p + C_n)\Delta n^2} \tag{5.13}$$

In the low injection limit the expression reduces to:

$$\tau_{Auger} \approx \frac{1}{C_p p_0^2 + C_n n_0^2} \tag{5.14}$$

In bulk silicon C_p and C_n are of order 1×10^{-31} cm^6/s.

The results quoted above are true in bulk Si. The question remains if VLS materials should behave as bulk materials. The answer to this question depends on the diameter of the VLS materials in question.

Consider a VLS wire with a very large diameter. Clearly in this limit the material is bulk like and the results do apply. As the diameter of the wire is reduced the ratio of surface atoms to bulk atoms increases. Although the number of states increases the nature of the surface states will largely be the same as the bulk case as these states are caused by localized dangling bonds at the surface of the Si. As the diameter continues to shrink quantum confinement will begin to affect the band structure of the material. The onset of this behavior can be estimated by the ratio of the confinement energy to the bandgap of the material. Taking nominally hexagonal VLS wires for simplicity to be square in

cross section this energy is twice the well-known 1-D result from quantum mechanics: $E = \frac{\hbar^2\pi^2}{mL^2}$. Taking L to be 10 nm for a free electron this energy is 0.0075 eV. Taking L to be 100 nm this energy is 7.5×10^{-5} eV. Given these estimates are correct to a geometric factor near unity, it is very safe to assume that transport in wires significantly in excess of 10 nm diameter is not affected by quantum confinement. The wires considered experimentally will all be in excess of 100 nm. Given that there are no quantum effects of significance for large VLS wires and no new trap mechanisms at the surface, the bulk results of Si can be applied to VLS wires without modification.

5.3 Methods of measuring carrier lifetimes

There are many ways by which the lifetime of a material can be measured. Schroder's chapter on carrier lifetimes [39] provides a good summary of the methods commonly used. Generally speaking the methods fall into two categories: device based methods and material methods. Capacitor and diode structures are the most common device structures used to measure carrier lifetimes. Device based methods such as these suffer from overhead in that one must fabricate a device each time to make the measurement. Fabrication of a device inherently is a modification of the material and the steps used to create these modifications affect the lifetime of the material. Thus device based measures are excellent for extracting physical parameters for modeling devices but less useful for understanding the intrinsic properties of a material. Finally device based methods require well behaved device characteristics to allow for correct interpretation. These drawbacks of device based approaches make their application less desirable for the purposes of studying the intrinsic material properties of

VLS wires.

Material based methods require either no device fabrication or very simple modifications such as electrical contacts. Based on the photovoltaic performance in chapter 4, and results published in the literature [37], sub-ns to ns lifetimes were expected for the VLS materials under study. Given these constraints I chose to pursue a measurement of VLS material based on a contactless measure of photoconductivity decay (PCD). This method is commonly used to measure materials rapidly for quality and is free of the need of any fabrication. It can be used to directly measure a material system's intrinsic carrier lifetime. Application of this technique to VLS wires however is not without challenges. Classic PCD experiments [41] [42] do not apply the technique to thin materials nor to materials with sub-ns lifetimes.

5.4 Microwave reflectance as a measure of conductivity

PCD can be viewed as a contactless measure of impedance or as a measure of reflected/transmitted microwave power. In Yablonovitch's work [42] the design of the experiment is best thought of as a RF impedance bridge in Kunst and Beck's work [41] the measurement is more easily understood as a measure of microwave reflectance.

In general when an electromagnetic wave strikes the boundary between two media part of the wave is reflected and part of the wave is transmitted. The fraction of each depends on the effective impedance mismatch at the interface. For an interface between two semi-infinite media the reflection coefficient is given by:

$$\Gamma = \frac{\eta_2 - \eta_1}{\eta_2 + \eta_1} \tag{5.15}$$

Where η is the impedance of the medium in ohms ($\eta = \sqrt{\mu/\varepsilon}$). For a finite medium the reflection coefficient must be modified to account for the extra boundary conditions imposed.

VLS materials have conductivity; it is in fact the measurement of this conductivity as a function of time that must be recorded in PCD. When a material has conductivity it is lossy and the permittivity of the material is commonly written as $\varepsilon_c = \varepsilon_r\varepsilon_0 + \frac{i\sigma}{\omega}$. Here the real term is the common permittivity for a non-lossy medium and the imaginary term is caused by the medium's conductivity. Through the complex permittivity the impedance of the medium also becomes complex. If the conductivity changes as a function of time so does this impedance and in turn the amount of reflected (and transmitted) electromagnetic radiation.

To modulate the conductivity of a sample PCD shines an above bandgap light pulse on the semiconductor. This creates electron-hole pairs (EHP) in the sample proportional to the number of incident photons. In bulk Si these EHP are broken apart thermally and create free carriers in excess of the thermal equilibrium populations. When the light is turned off this population relaxes to equilibrium. It is this relaxation that is measured as function of time via PCD which is inferred through a measure of the change in the microwave interaction with the sample (i.e. reflection).

From this conceptual picture of PCD requirements for the method are already apparent. To measure fast recombination the light pulse must be faster

than the recombination or of a precisely known shape which could be deconvolved in principle from the data taken. Second the light must create enough EHP to change the amount of reflected microwaves measurably. In bulk materials PCD is considered a surface method because as the conductivity increases there is a skin depth that the microwaves can penetrate. For thin films of materials the method probes the entire volume.

5.5 Sample structure

Having covered the basic concept behind PCD the next consideration for designing an appropriate means of measuring a sample of VLS material is the structure of the sample itself. For this work epitaxial wires were used as these wires have the highest possible material quality. This naturally means the VLS materials are created on a single crystal substrate. This wafer has its own lifetime and transport properties which are not the subject of the investigation. It is likely that this substrate would have a lifetime greatly in excess of the VLS materials. If the VLS wires were left on this substrate and measured this substrate would effectively become metallic and stay metallic long after the VLS material had fully relaxed. Such a planar metallic layer would reflect nearly all microwave radiation making it almost impossible to see any signal due to the VLS materials. Therefore the wires must be removed from the growth substrate onto a carrier material which is not conductive to perform this measurement. For this purpose fused silica was used. The wires were removed mechanically into alcohol and repeatedly centrifuged to densify the alcohol suspension. This solution then was placed on the fused silica and allowed to dry. This creates a thin film of VLS material with air gaps between the wires as can be seen in

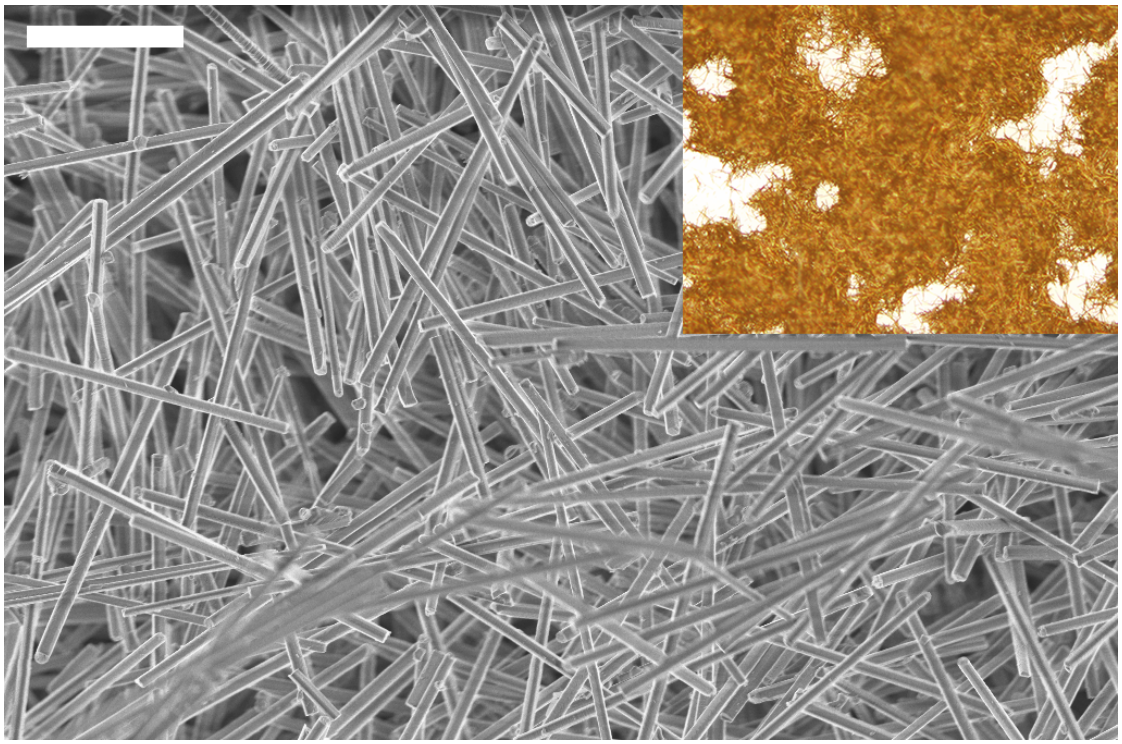

Figure 5.1: Two views of Au-Lith1 sample showing the porous nature of the wire film. The scale bar in the SEM is 10 μm, the field size of the optical micrograph is not known. It shows there are mm size gaps in the wire film in addition to the micron scale gaps seen in the SEM.

Figure 5.1. The air gaps have important experimental consequences which are discussed later in this chapter. For the purpose of discussion for now I will take the sample structure to be a thin micron scale semiconductor film on a fused silica support. Thus when light is pulsed EHPs will be created in the thin film of wires which can be monitored via PCD.

5.6 Design of the PCD instrument

Design is a series of tradeoffs. From the above discussion it is clear that the most important feature of the instrument is that it must be able to monitor the con-

ductivity of a thin film on a time scale less than 1 ns, preferably much less. The light source used must inject carriers much faster than this and inject enough carriers to see. In addition to a fast light source a source of microwave radiation is needed. Given the one time use of this design purchasing expensive lasers and sources was not conceivable. Therefore the next step in the design process was to consider what was available. Fast lasers are common at Cornell, though as will be seen there are more considerations than just speed. Microwave sources were also available through the Center for Nanoscale Systems, as were fast oscilloscopes capable of direct single shot sampling of waveforms up to 11 GHz. Because direct sampling of the carrier wave is a possible means of detection I began my experimental design with this frequency as the upper bound of the microwave radiation used to detect the conductivity. Having studied the literature on the subject I decided on an approach similar to Kunst and Beck's work [41] and to suspend the sample in a waveguide. The most appropriate choice for this waveguide given commonly available microwave parts seemed to be an X-band WR-90 waveguide.

The prior conceptual discussion of the microwave sample interactions now must be considered in detail. Factors that potentially must be included are the sample's location inside a waveguide, the wire film's porosity, the fused silica support, absorption coefficients of the wire film and potentially its linearity. In the context of these factors a means of detection must be constructed which is fast, sensitive and low enough noise to see the desired effect.

Placing a media in a waveguide modifies the material's impedance and the propagation constant:

$$\eta = \frac{\eta_{free}}{\sqrt{1 - (\frac{f_c}{f})^2}} \tag{5.16}$$

$$\gamma = ik\sqrt{1 - (\frac{f_c}{f})^2} \tag{5.17}$$

Here η_{free} is the impedance of the material in free space, k is the wavenumber of the microwaves, f_c is the cutoff frequency of the waveguide in the TE mode, and f is the frequency of the microwaves. To calculate the reflected amount of microwaves the previously defined complex dielectric constant must be used to obtain the wavenumber $k = \omega\sqrt{\mu_0\varepsilon_c}$. Finally the finite thicknesses of the materials must be accounted for. For a single finite film (media 2) bounded by vacuum (media 1) the reflectance is:

$$\gamma = \frac{-2\sinh(\gamma_2 d)(\eta_1^2 - \eta_2^2)e^{-\gamma_2 d}}{e^{-2\gamma_2 d}(\eta_1 - \eta_2)^2 - (\eta_1 + \eta_2)^2} \tag{5.18}$$

In the limit that the film appears thin given its impedance ($\gamma d \ll 1$) this becomes:

$$\gamma = \frac{\gamma_2 d(\eta_1^2 - \eta_2^2)}{2\eta_1\eta_2} \tag{5.19}$$

The analogous expression for reflectance from two finite films was used to estimate the reflected power for the experiment. This expression has significantly more terms than the above without any additional elucidative value and so is omitted here. However results of its application are plotted in Figure 5.2.

The results are in essence a Bode plot. Inspection shows that in the single film case the lower asymptote is provided by the real part of silicon's dielectric constant. The upper asymptote is formed when the Si becomes metallic. Being Bode-like the addition of the fused silica support slide compresses this function by addition on the log scale. The most notable deviation from this intuitive picture of the reflectance-carrier density transfer function is the small dip as the complex part of the dielectric constant becomes comparable in size to the

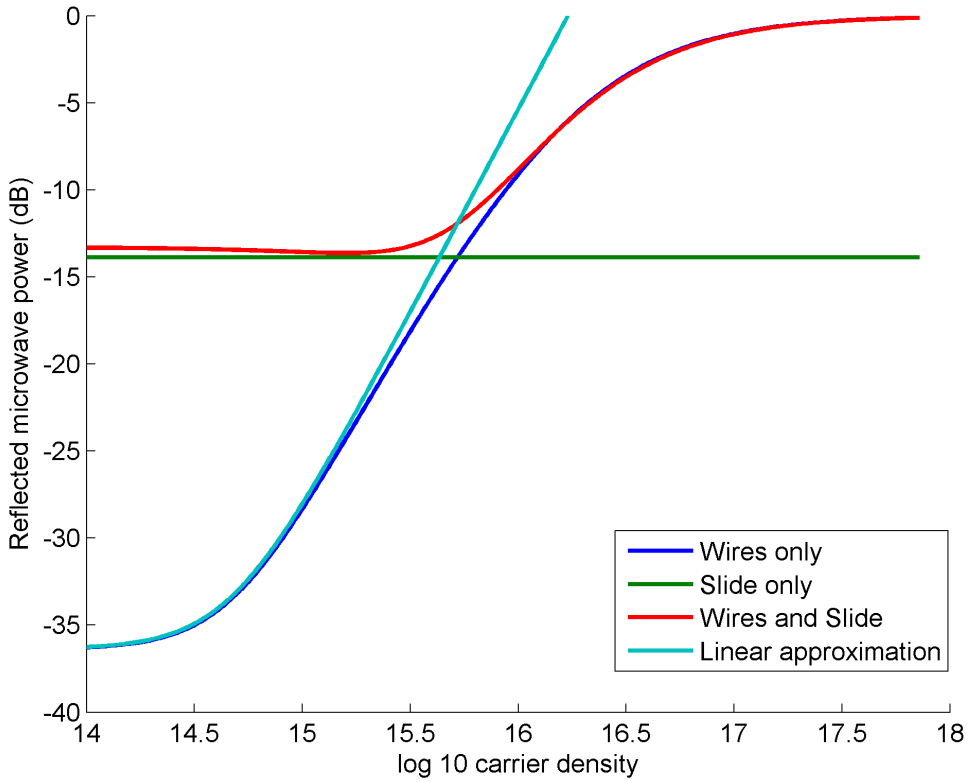

Figure 5.2: This figure shows the calculated attenuation of reflectance from a thin film stack consisting of 1 μm thick Si film and/or a 500 μm thick SiO_2 slide. Also shown is a linear approximation to the Si thin film alone. These results provide guidance for the needed injection level to observe a signal at any SNR. The actual behavior includes effects related to the porosity of the film not included in this calculation.

real part. In this region the reflectance decreases due to a standing wave in the composite material thickness. Because the material impedance is complex this resonant effect is non-singular. These general qualitative characteristics will be true for any chosen thickness of the conductive thin film and support slide. The magnitude of the effects depends intimately on the chosen geometry. Comparison of the specific calculation to a linear approximation shows significant deviation from agreement due to the support slide's compressing effect covering up the perturbative region. Finally the calculation provides insight into the magni-

tude of detectable power that will be reflected. Although the exact magnitude of carrier injection needed will depend on the sensitivity of the detector used, this simple model predicts an injection level of 1×10^{18} to 1×10^{19} carriers per cubic cm should provide full swing. From this value the needed pulse power of various lasers can be estimated. Most of the available fast pulsed lasers at Cornell at this time are based on Ti-Sapphire oscillators and so the needed pulse power is appropriate to estimate in the near infrared. Taking the wavelength to be 800 nm the bulk linear absorption coefficient for Si is 936/cm [43]. For a 1 μm thick sample this equates to nominally 9% absorption. Thus the photon count needed per pulse is 1 order of magnitude larger than the carrier density. Photons at 800 nm have an energy of 1.55 eV or 2.48×10^{-19} J. From these values it is clear a pulse energy on the order of 100s of mJ may be needed to modulate the sample. Searching for a laser that met this requirement I found that Prof. Chris Schaffer had a regenerativly amplified Ti-Sapphire laser with a pulse power of 600 mJ and a pulse time of 100 fs. This laser met both the temporal and power requirements provided by these estimates. Prof. Schaffer was gracious to allow me to use it with the help of his student Andrew Davis.

The final part of the system needed is a detector of the reflected power. As noted earlier direct sampling at the frequency used is technically possible. Other schemes involve AM detection either by a fast rectifier, heterodyne receiver or a direct-conversion (homodyne) receiver.

Diodes with recovery times fast enough are available however when integrated most offer a limited video bandwidth not wide enough for the predicted signals. This leaves heterodyne and homodyne detection based on wide bandwidth mixers. The latter requires fewer sources and has lower phase noise and

was selected as the means of detection.

The preceding discussion was provided so that the reader may understand some of the trade-offs that were made in constructing this instrument. Some of them are non-optimal. In fact if the system were designed again a significantly higher microwave frequency would be advisable. Given that direct sampling was not employed in detection this would have reduced ripple in the final signals and allowed for more efficient use of the VLS materials as the waveguide area would have decreased.

5.7 Final instrument description and operation

The final instrument design can be seen in Figure 5.3. In this system, the sample under study is suspended in a WR90 waveguide which is matched to the room with a microwave horn. This ideally allows the fused silica/wire sample to be treated as a single impedance mismatch inside a semi-infinite waveguide as was considered earlier. A 10 GHz microwave tone at a power of 24 dBm is applied to the system through a -6 dB directional coupler used as a power splitter. The through port of the directional coupler is attached to a ferrite circulator which passes the tone to a waveguide coupler. The continuous wave passes down the waveguide and is partially reflected from the sample with the rest of the microwave power passing out of the horn and into the room. This arrangement makes the setup sensitive to materials outside of the waveguide as well. In particular metallic objects need to be kept far away from the end of the horn to avoid reflecting considerable microwave power back into the waveguide. For this reason dielectric mirrors were employed on fiberglass posts to

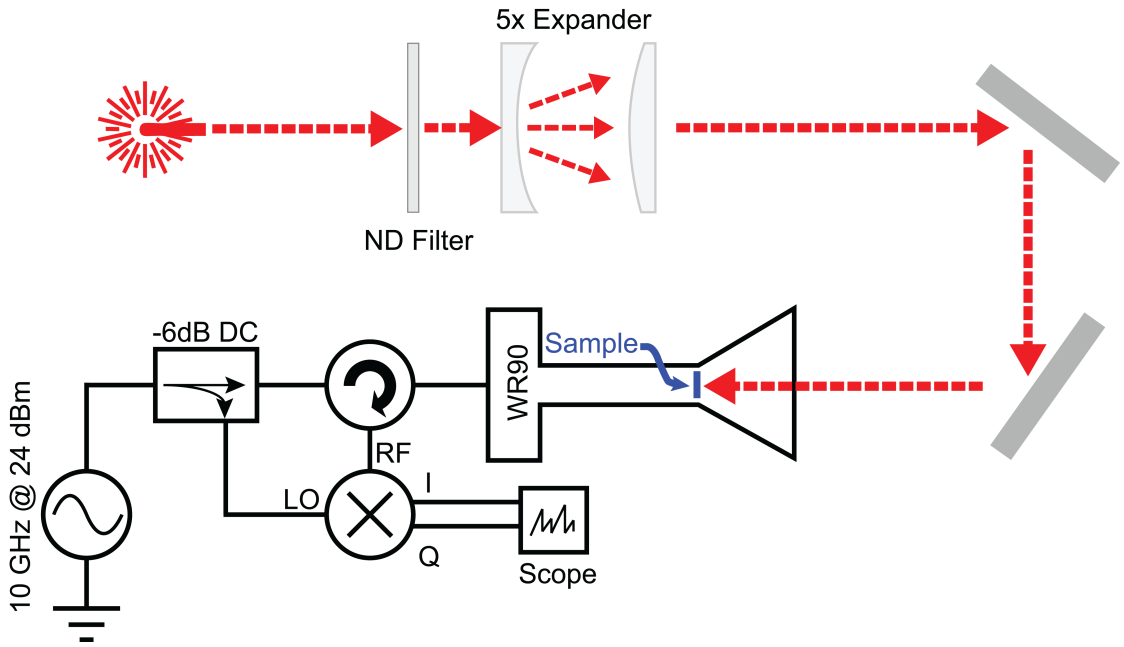

Figure 5.3: A 1 KHz repletion rate regeneratively amplified Ti-Sapphire laser at 800 nm generates 100 fs pulses with a peak power of 600 mJ per pulse. These pulses pass through a selectable ND filter and then are expanded via a 5X Galilean beam expander. The pulse is routed via dielectric mirrors down a microwave horn and onto the sample which is suspended in a WR90 waveguide. A microwave tone at 10 GHz at 24 dBm is generated by a YIG based CW sine source. This power is split by a -6 dB directional coupler, the coupled port is attached to the LO port of an IQ mixer and the through port to a ferrite circulator. The circulator forwards the power to the waveguide via a SMA to WR90 coupler. The reflected power is AM modulated by the conductivity change in the sample caused by the laser pulse. The reflected power is sent to the RF port of the mixer via the circulator and demodulated into its phase quadrature components: I and Q, which are recorded by an oscilloscope.

route the pulsed laser onto the sample. This pulsed laser injects excess carriers into the semiconductor wires, which changes their conductivity. This conductivity relaxes after the pulse. The relaxing conductivity continuously changes the impedance mismatch in the waveguide. This produces an amplitude modulation (AM) on the reflected carrier wave. The reflected wave is separated from the incoming wave by the ferrite circulator and passed to the radio frequency (RF) port of a phase quadrature (IQ) mixer. The reflected wave's AM is detected

by the IQ mixer used in a homodyne arrangement and recorded using an oscilloscope to give a measure of the voltage reflectance as a function of time. This detection arrangement has a measured 3-dB bandwidth of better than 1 GHz. Any pulse measured with this detector represents the convolution of this detector's response with the pulse shape.

Carrier injection is achieved via the previously mentioned regeneratively amplified mode locked Ti-Sapphire laser. The laser had a repetition rate of 1kHz, a pulse energy of 600 mJ, and a wavelength of nominally 800 nm. Regeneratively amplified lasers such as the one used are often used for non-linear optical experiments. Here non-linear absorption effects are undesirable. Meanwhile uniform illumination of the wire film is desirable. Both aims benefit from expansion of the laser beam. In the present case the $1/e^2$ beam diameter was expanded to 25 mm. Given the unattenuated pulse power this equates to a peak flux of 10 GW/cm^2. For silicon, at this flux and wavelength, linear absorption dominates [44] [45].

5.8 Discussion of raw instrument data

After building an instrument one must always be careful to understand any systematic effects that exist before applying it to the desired measurement. I completed measurements of bulk Si first, and the results agreed well with historical PCD measurements. After this I applied the system to VLS films on fused silica. The details of these VLS materials will be covered in the experimental results section later in this chapter. For now consider the data in Figure 5.4 as typical raw data provided by the instrument. As can be readily seen the data

is not a simple single peak with a subsequent decay, rather it is a set of peaks. Both the optical system and the microwave system contribute extra peaks. In Figure 5.4 the peaks marked in red are from the laser and the peaks marked in blue are from the microwave system. The output of the laser is actually a pulse train. This train consists of a set of pulses at the mode-locked frequency of the oscillator that drives the regenerative amplifier. These extra pulses have significantly less power than the primary pulse released each millisecond; however they appear clearly in the output because the detection scheme is sensitive to many orders of magnitude of carrier injection as was seen in the theoretical calculations earlier in this chapter. To understand the source of the extra peaks caused by the microwave part of the system consider again the instrument diagram in Figure 5.3. The system consists of multiple components strung together. Each of these components has an imperfect impedance match to the next. This causes a standing wave to build up between any two parts as a function of time. This is typically parameterized as the voltage standing wave ratio (VSRW) in datasheets. This standing wave builds up in time domain after many reflections back and forth, thus the propagation time of the wave is relevant to this effect. Here the peaks in blue are from the VSRW of the waveguide coupler and the sample. The time between the primary light pulse and the echo of that pulse is 7.8 ns. In a 50 ohm system this represents a distance of 0.31 m. This is twice the length of the waveguide section used, thus the echo is from a pulse that reflects from the coupler and the sample and adds to the reflected power after returning to the sample.

The last item of note in the example raw data is that there are two types of decay in the sample. A fast decay and a very slow background decay. This background decay is in fact slow enough that it does not completely relax in a

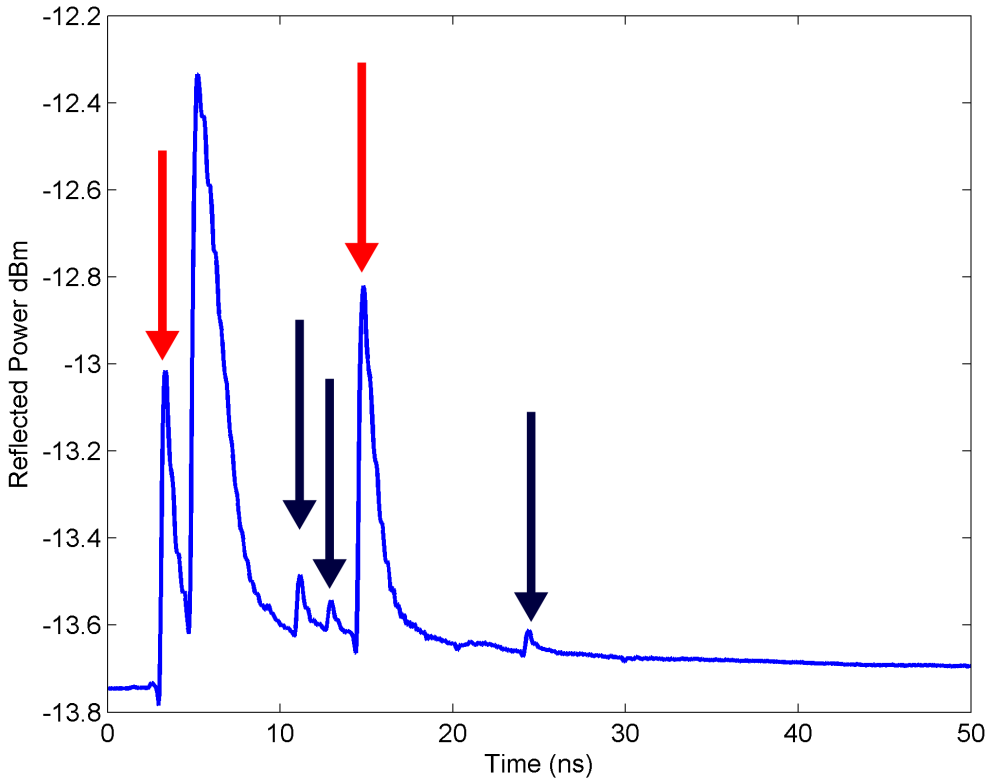

Figure 5.4: The reflectance data created by the instrument contains systematic artifacts from both the laser and microwave systems. The laser does not release a single pulse at $t = 0$ instead it releases a train of pulses at the master oscillator repetition rate. These pulses marked with red arrows are significantly less powerful than the main pulse but due to the very large dynamic range of the instrument are easily visible. The microwave system via impedance mismatches, primarily at the microwave coupler and sample interfaces has a non-ideal VSRW resulting in a building standing wave, marked in dark blue. This can be seen in time due to the fast readout of the instrument.

millisecond time scale. This fact was observed by attenuating the laser which shifts power reflected by this quasi-static level. The question therefore is which decay represents the VLS material properties that are the objective to study with this instrument? The answer is the fast decay. It is known from the production of photovoltaics that VLS material does not have a lifetime on the order of milliseconds. If they did their performance would be excellent given their dimensions.

What then is the source of this slow decay? Although there are several reasons such a slow decay could exist in the sample the most reasonable is charge traps located at the wire surface. Such traps would be able to release carriers proportional to their original population slowly and thus affect the conductivity. One means to test this hypothesis would be to vary the temperature of the sample, however this was deemed impractical given the instrument design.

The final question to consider given the raw data collected is how to extract the material lifetime from it. Typical PCD measurements attempt to relate the measured reflectance signal to the absolute conductivity through a model. This approach makes sense in a sample that is well defined geometrically and is spatially homogeneous. The wire samples are not spatially homogeneous on a micron scale (Figure 5.1). However, on the scale of the coupled microwave signal they are. This assures that the microwave sees a single effective impedance mismatch in the waveguide. However, this sub-wavelength inhomogeneity does change the effective dielectric constant that the microwave interacts with. This complicates modeling. An effective medium theory [46] [47] could be used to construct a model of an aggregated wire film if it was sufficiently characterized. However, such a lengthy characterization would defeat the aim of the instrument: simple rapid assessment of material quality. Because of this, a much more direct approach was employed. The intensity of the laser light was varied to directly change the relative carrier densities injected in the samples. From this the unknown transfer function between injected carrier density and reflectance can be inferred.

5.9 Lifetime extraction method

Consider a PCD experiment with a laser that creates N EHP at $t = 0$ in a semiconductor sample with a reflectance transfer function $\Gamma = g(\sigma)$, where σ is the effective sample conductivity. If $N \gg N_a, N_d$ then as the sample relaxes toward equilibrium $N = N_e = N_h$ where N_e electron density, N_h is hole density, N_a is the acceptor density, and N_d is the donor density in the sample. This condition is high level injection. In this case $\sigma = eN\mu$ where μ is the sum of the electron and hole mobilities. This means that in the high injection limit the conductivity is solely a function of N. The mobility also varies but it too is only a function of N for a fixed sample at a fixed temperature.

This allows the definition of another reflectance transfer function $\Gamma = h(N)$. If this function were known then a measure of reflectance would directly indicate the free carrier density in the sample at any time as it relaxes. Thus a measurement of reflectance would be a measure of the carrier lifetimes.

This transfer function can be measured experimentally. Consider two light pulses A and B with two different powers P_A and P_B, but otherwise identical, incident on a sample. If the absorption of the material with respect to light intensity is linear then the ratio of the maximal number of EHP in the material from the two pulses is equal to the ratio of the light pulse powers, that is: $\frac{P_B}{P_A} = \frac{N_B}{N_A}$ at $t = 0$. This gives two points on the transfer function. By using many different intensities the entire function could be reconstructed except for a constant because of the differential nature of the mapping. This constant can be added to the function either by an experimental estimate or it could be removed from the experimental data numerically.

The method just described conceptually summarizes how to reconstruct the lifetimes without a model using just reflectance data and light pulses of different intensities. To be mathematically exact such a reconstruction needs to be differential in nature with a continuous differential variation in light pulse power. In practice this is of course not possible with a finite number of measurements. A suitable method to achieve this same objective is to measure the relaxation time between pairs of pulses that inject different carrier densities. This allows the average recombination rate to be measured between two relative carrier densities.

Again, consider the two pulses. To make things simpler, assume the recombination process is purely first order. In that case, $N(t) = N_0 e^{\frac{-t}{\tau}}$. Then let $N_B = N_A e^{\frac{-t_1}{\tau}}$ from this it follows that $\tau = \frac{t_1}{ln\frac{N_A}{N_B}} = \frac{t_1}{ln\frac{P_A}{P_B}}$. In this thought experiment, t_1 is the time it takes the carrier density to relax to N_B after pulse A. Equivalently, it is the time that it takes the reflectance Γ to relax to the amount of reflectance created by pulse B at $t = 0$. Thus, t_1 can be measured by measuring the reflectance as a function of time for two light pulses of different powers. Meanwhile, the power of each pulse can be measured directly using a power meter. From these two measurements the lifetime τ of the sample can be extracted.

If the recombination process is not purely first order then the lifetime measured is the time constant of the exponential needed to match the carrier density at $t = 0$ and $t = t_1$. The differentially small version of this method can build up the entire recombination rate curve versus carrier density in the high injection level limit. As noted earlier in this chapter in terms of Hall-Shockley-Read (HSR) theory this high injection lifetime is: $\tau = \tau_n + \tau_p$ where τ_n, τ_p are the electron and hole minority carrier lifetimes respectively.

In this procedure it was assumed that the materials' absorption is linear. This

assumption should be checked experimentally for each sample and any deviation accounted for.

This method is sufficient to study the relative lifetime as a function of injection level. To compare samples it is necessary to know the absolute injection level of the sample. This can also be directly measured: by combining measurements of the sample's active volume with measurements of the samples absorption. This data provides an absolute scale to the carrier density and thus the missing constant of the differential technique described.

5.10 Methods for experimental determination of lifetimes in vapor-liquid-solid wires

To provide pulses of different intensities but identical shape a set of reflective neutral density (ND) filters in half order of magnitude increments was used to attenuate the laser. By measuring the reflectance created by each one of these pulse intensities the differential measurement described in the preceding section is achieved. The result of this method is a family of curves for each sample measured by the reflectance instrument. An example of such a family of curves is shown in Figure 5.5. The traces shown are taken from the time between the principle light pulse in the laser pulse train and first echo from the waveguide VSRW. This region is free of artifacts and can be directly compared between samples; the ripple seen in the traces is from feedthrough of the up-converted microwave carrier (caused by the finite isolation of the mixer).

As noted to determine the absolute injection level an estimate of both the

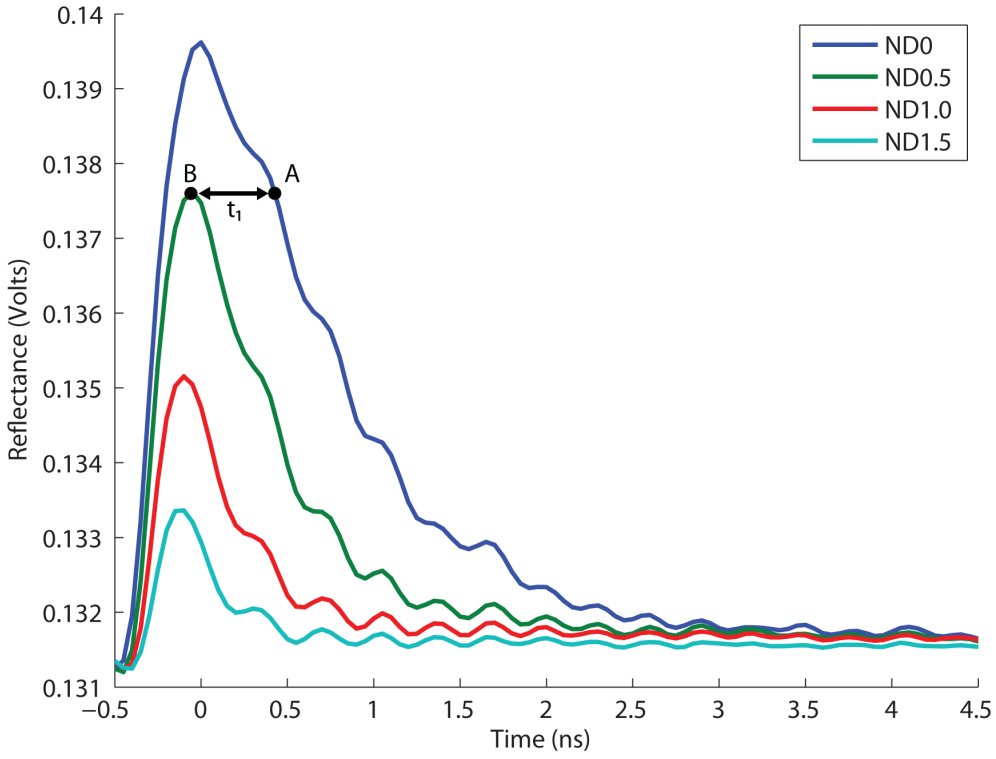

Figure 5.5: A typical family of reflectance traces from the experimental apparatus, in this case for sample Au-Lith2. The pulse attenuation caused by each ND filter is known via a power meter measurement. The ripples are from the up-mixed frequency component which is not completely filtered. To measure the time between A and B each curve is fit to an exponential decay and the time offset calculated.

sample volume and absorption is required. A simple estimate of the active volume may be made by knowing the wire density and sample size before the transfer process, and assuming some transfer efficiency. A transfer efficiency of 100% places an upper bound on the active volume. Direct inspection of the 2-dimensional coverage of the carrier fused silica, combined with scanning electron microscope (SEM) and transmission electron microscope (TEM) measurements of the wire diameter provides a lower bound estimate of the active volume (any covered area has at least one wire layer). A more accurate estimate of the volume can be made by combining SEM/TEM observations of the wires

and wire film with profilometry, to estimate the film porosity, wire size and film thickness. If higher accuracy is needed measurements of the sample volume might also be made using a crystal mass sensor. For the present work a combination of SEM, TEM and profilometry measurements along with the bounding estimates described were used to calculate the active volume.

In the present experiment a Shimadzu UV-3101PC spectrophotometer was employed to measure the reflected and transmitted power, and thus the absorption. The transmitted power was compared with the measured transmitted power of the high power experimental laser with a Coherent FieldMax II/PM3 thermopile sensor, to verify the linear absorption assumption for each sample, with any deviation added to the error in the reported lifetime.

These methods were applied to 5 samples. The 5 samples represent two experiments. The first experiment is a measure of the dependence of the lifetime of Au catalyzed VLS wires as a function of diameter. This experiment consists of lithographically defined wires of 3 different diameters co-grown and co-processed at all steps. The second experiment consists of two samples grown from thin metal films, one grown from Al the other from Au. The objective of this experiment was to observe lifetime differences cause by the catalyst type.

5.11 Material growth and sample preparation details

The lithographic samples were created using the standard oxide liftoff method described in chapter 2. The pattern consisted of 1 μm diameter Au islands defined in a square array with 2 μm pitch. Three thicknesses of Au were used 19, 63, and 155 nm. These samples had the liftoff oxide removed in HF 10:1 prior

to being loaded in the UHV-CVD reactor at IBM. The three sample types were then annealed under UHV conditions for 10 minutes at 750 C. SiH_4 was turned on for 25 minutes at a pressure of 250 mTorr at 750 C then the temperature was reduced to 650 C over 10 minutes with the SiH_4 flow rate and pressure kept constant. At 650 C the wires were allowed to grow for 295 minutes at 250 mTorr.

The initial higher temperature step is necessary to reduce kinking at the wire base for these large diameter wires. After the growth was completed the Au catalyst was removed using KI/I_2 Au etch. The wires were then washed in DI, dipped in HCl, and then washed in DI again. After this the samples were oxidized in a dry oxygen atmosphere at 950 C for 12 minutes. The intention of this oxidation step was to passivate the surface of the wires. The resulting wires were nominally 23 μm in length. The resulting silicon diameters were 730, 577 and 392 nm for 155, 63 and 19 nm thicknesses respectively as measured via combined SEM and TEM observations.

The Au-Film and Al-Film samples were grown on <111> Si wafers as well. These wafers were simply dipped in HF before having a thin Al or Au film deposited on them. The Au film was deposited to a thickness of 2 nm in a separate evaporator while the Al film was deposited in-situ in the CVD tool in UHV conditions to a thickness of 8.5 nm.

The Al-Film sample was annealed 20 minutes at 750 C, then cooled to 490 C. A mixture of SiH_4 (10 SCCM) and B_2H_6:He (1000 PPM B_2H_6, 1 SCCM) was then flowed in the chamber. This flow was maintained at a reactor pressure of 550 mTorr for 60 minutes, after which the B_2H_6 was turned off. With the B_2H_6 turned off the wires were grown 180 minutes longer at 550 mTorr and then removed from the chamber. The Al catalyst was removed with HCl, and

the wires were oxidized at 1000 C in a dry oxygen atmosphere for 25 minutes. The intention of this oxidation step was to passivate the surface of the wires. The mean wire silicon diameter for this growth was 144 nm as measured via combined SEM and TEM observations.

The Au-Film sample was redipped in HF 10:1 prior to loading into UHV, having been exposed to air after the Au evaporation. It was annealed at 600 C for 10 minutes. The chamber was then pressurized to 200 mTorr with SiH_4 and the wires were grown for 120 minutes. After the growth was completed the Au catalyst was removed using KI/I_2 Au etch. They were then washed in DI, dipped in HCl, and then washed in DI again. The wires were oxidized at 1000 C in a dry oxygen atmosphere for 25 minutes. The intention of this oxidation step was to passivate the surface of the wires. The mean wire silicon diameter for this growth was 125 nm as measured via combined SEM and TEM observations.

The different reactor conditions between the Au-Film and Al-Film growths are necessitated by the different phase diagrams of Au-Si and Al-Si. The goal of the sample pair was to create wires of similar diameter to control for surface states, and thus isolate the catalyst metal as the effect. In practice however, the growth rate of Al catalyzed wires is slower than their Au counterparts. This means the taper of the wires is different and thus their surface areas, even for wires of the same mean diameter. This taper is caused by the ratio of the side-wall growth rate to the catalyzed growth rate. The absolute diameter of the wires is sensitive to both the anneal time, temperature and film thickness.

Fused silica chips were cut with a diamond dicing saw to the size of a WR90 waveguide. To transfer the wires to this substrate, the growth wafer for each type was placed in a clean Pyrex dish, covered in a thin layer of isopropanol

(IPA) and brushed with the edge of a microscope slide. This breaks the wires mechanically near their base. The IPA containing the wires was transferred from the Pyrex dish into eppendorf tubes and centrifuged. This results in a pellet or dense liquid near the bottom of the tubes. The more clear top solution of the tube was removed via a pipette and the number of tubes and solution volume reduced. The reduced solutions were remixed before combining the solutions of the tubes together. Once the volume was reduced to a few mL the solution was dispensed on the fused silica chip and slowly allowed to dry. This results in a powder like aggregated wire film on the fused silica surface. This film ranged in thickness between 5 and 20 μm in thickness for the samples described here.

5.12 Experimental results

The results of the experiment are summarized in Table 1. Meanwhile the samples lifetimes are compared at a nominal injection level of 4×10^{17} EHP/cm^3 in Figure 5.6. The samples are compared at this relatively high injection level because of the strong *p*-type doping of Al catalyzed wires (caused by Al as an acceptor), and high injection level requirement.

The errors reported and plotted in the diameter represent both the spread in the measured diameter across the ensemble as well as the taper of the wires from the base to the tip. The taper is a result of conventional CVD processes occurring in parallel with the VLS type growth. This conventional CVD growth occurs on the sidewalls of the wires as well as the spaces between them with a rate and quality similar to the conventional planar CVD that would occur under identical reactor conditions.

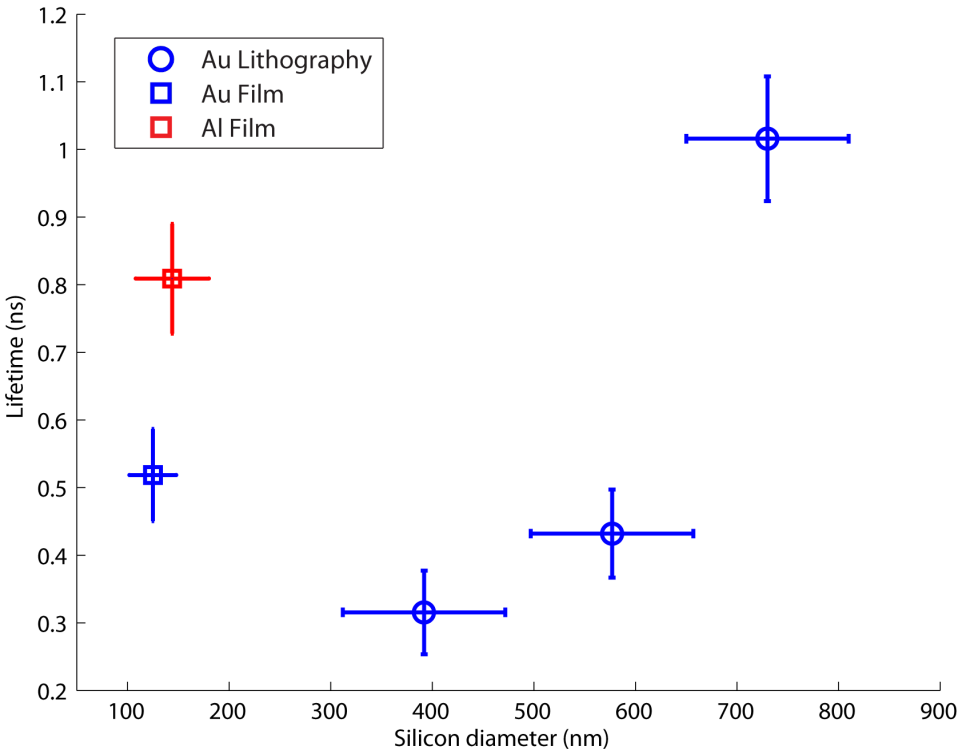

Figure 5.6: Comparison of carrier lifetimes across samples at a nominal injection level of 4×10^{17} EHP/cm^3. The lifetimes seen are linearly interpolated for this injection level using the data in Table 4.1, namely the relative ND based carrier lifetime and the nominal EHP injection level.

The errors reported and plotted for the lifetime represent the errors from the time base and trigger jitter of the oscilloscope, absorption measurements, and power detector measurements, as well as the random error of the detected signal.

From the data several observations are immediately clear. First, in the 3 samples meant to compare the effect of diameter on lifetime a strong dependence on diameter is observed. Second, Al catalyzed wires are not significantly superior to their Au counterparts. Third, although the injection levels used are high, Auger processes may be ignored. (The bulk Auger coefficient for Si is less than

1×10^{-30} cm^6/s resulting in an effective lifetime greater than 10 ns at an injection level of 1×10^{19} EHP/cm^3). Thus, we may consider only defect mediated recombination processes both at the surface and in the bulk.

Consider the 3 co-processed Au samples with lithographically defined islands (Au-Lith1,2,3). In the data shown in Figure 5.6, we see a very strong dependence on diameter. This strongly indicates that surface or near surface processes are the dominant sources of recombination even in these relatively large diameter VLS wires. In fact these data completely preclude the commonly held view that bulk Au contamination is the principle reason for the relatively low lifetimes of VLS materials. Because these samples were grown together and processed together in all steps if bulk Au was the dominate recombination mechanism all of their lifetimes would be approximately equal, which is not the case.

The cause of the surface area dependent recombination in these samples is not clear from these data however. There are several possible and indistinguishable sources of recombination in these samples that may appear as surface like terms: traditional surface recombination at the Si/SiO_2 interface, recombination from enveloped Au near the surface, and lower lifetime sidewall material.

Traditional surface recombination caused by defects at the Si/SiO_2 interface, is certainly present and unavoidable in these samples. This mechanism should be approximately equal per area on each sample given they were all passivated with the same high temperature thermal oxide. If this were the only mechanism the data should fit a simple two parameter theory with a surface recombination velocity and a bulk lifetime. For the data in Figure 5.6 such a theory is a poor fit. Attributing all of the recombination in each wire sample to surface processes

can give an upper bound on the surface recombination velocity. Doing this for the data in Figure 5.6 results in surface recombination velocities ranging from 2×10^4 cm/s to 4×10^4 cm/s. These values are significantly in excess of what is expected for a thermal oxide passivation (≈ 100 cm/s) [42]. Both of these facts are suggestive that other mechanisms are likely present.

Au is known to migrate along wire sidewalls in UHV conditions [22]. The exact Au sidewall coverage appears to be a function of reactor conditions [17]. During a typical VLS wire growth regular CVD processes are occurring in parallel with the VLS mechanism resulting in wire taper and the accumulation of regular CVD material on the wire sidewalls. While this sidewall Au may remain on the surface at all times (as the catalyst does), it cannot be ruled out that the sidewall growth envelops some of this Au with Si. As the wire diameter decreases this could create an Au concentration greatly in excess of the solid solubility at the temperature used. More importantly it would appear as a surface like term with the Au localized near the surface. This Au would not be removed by the KI/I_2 Au etch used to remove the catalyst because of the Si covering it.

The surface term could also arise simply from the radial growth. The material that grows on the sidewall, although clearly epitaxial given the faceted nature of the resulting wires, may simply be more defective in terms of crystalline defects than the VLS core of the wire [48]. Because the sidewall material grows at a rate that is essentially a constant radial thickness per time there is a greater ratio of sidewall to bulk material on wires that have a smaller diameter. Thus any deleterious effect of this material would affect wires of smaller diameters more. We are not able to distinguish the sidewall material from the core

Samples	Au-Lith1	Au-Lith2	Au-Lith3	Au-Film	Al-Film
ND0.0-ND0.5 Lifetime (ns)	1.00±0.09	0.45±0.07	0.56±0.07	0.69±0.08	0.81±0.08
ND0.5-ND1.0 Lifetime (ns)	0.98±0.09	0.42±0.06	0.35±0.06	0.52±0.07	
ND1.0-ND1.5 Lifetime (ns)	0.39±0.06	0.23±0.06	0.27±0.06		
Wire Diameter (nm)	836±79	655±71	492±104	245±23	200±36
Nominal ND0 Peak EHP Density (#/cm^3)	9.6×10^{17}	1.2×10^{18}	2.9×10^{18}	8.3×10^{17}	1.3×10^{18}
Upper Bound ND0 Peak EHP Density (#/cm^3)	3.3×10^{18}	3.2×10^{18}	5.2×10^{18}	8.1×10^{18}	8.3×10^{18}
Lower Bound ND0 Peak EHP Density (#/cm^3)	2.7×10^{17}	3.1×10^{17}	1.9×10^{17}	5.1×10^{17}	1.2×10^{18}

Table 5.1: Summary of lifetime results using the attenuated pulse PCD method.

wire in TEM observations; however we are able to place a bound on the thickness of this material based on the wire taper (Table 5.1). This material thickness has no thickness at the wire tip and may increase to a thickness as great as the reported upper bound at the wire base.

Now consider the two film based samples (Au-Film and Al-Film). From the data we see there is an improvement for Al catalyzed wires over their Au grown counterparts. However, one must consider the added complexity of using in-situ Al evaporation when deciding between Al and Au catalyst types. The data here may understate the advantage of Al catalyzed wires. As shown in the diameter dependence experiment surface effects are dominant, not bulk effects, so if these surface effects could be fully mitigated then Al catalyzed wires could indeed be superior. However, it is currently difficult to grow large diameter Al wires. This means that suppressing these surface effects is a significant

challenge for the Al-Si VLS system. Until this is accomplished simply growing larger diameter Au wires is likely to achieve better overall lifetimes.

It is tempting to compare the Au-Film and Au-Lith samples however they are not directly comparable. The Au-Film sample was grown at lower temperatures than the Au-Lith set. This results in a lower growth rate of both the wire and sidewall material. In the Au-Film sample more of the sidewall material was oxidized in the passivation step and the passivation oxide was grown at higher temperatures. These differences prevent a close comparison between the Au-Film and Au-Lith samples. However the lifetime of the Au-Film sample is longer than one might expect based on the Au-Lith data. Note that due to oxidation over half of the wire length in the Au-Film sample is free of sidewall material, which when combined with the Au-Lith data is suggestive that this material may be playing a prominent role in the recombination in this system.

5.13 Summary

Lifetime determination is important for assessing electronic quality of materials for applications where the bipolar characteristics are important such as in minority carrier devices, including *pn* junction photovoltaics. A conceptually simple extension of the PCD method allows the determination of carrier lifetimes of VLS wires. The procedure for measurement is simple: transfer the material to a transparent insulator; measure the microwave reflectance transient to at least two light pulses of different intensities and the power of the pulses; from this obtain the average first order lifetime for the mean injection level; obtain the absolute carrier density by measuring the samples absorption and active volume.

The experimental method used in this chapter while rapid and simple conceptually, requires costly equipment to implement. It also works in the high injection level limit which while providing useful data on carrier lifetimes is not the regime of normal photovoltaic cell operation. An alternative frequency domain method that addresses these issues is discussed in Appendix A.

Employing the extension to traditional PCD discussed in this chapter to study VLS materials shows that surface and near surface effects dominate recombination in Au catalyzed wires, and are the reason for the short lifetimes of these materials. In turn these short lifetimes explain the poor performance of these materials in photovoltaic applications. Al catalyzed wires may have a slight advantage over their Au counterparts; the effect however is not dramatic. This slight advantage of Al over Au is of limited value if a larger diameter Au catalyzed wire can be used in place with equal efficacy.

CHAPTER 6

SILICON NANOWIRE ATOMIC FORCE MICROSCOPY PROBES

6.1 Introduction

Scientific instruments are generally extensions of human senses. The familiar optical microscope and telescope extend human's dominant sense: vision. The electron microscopes used in this thesis, both SEM and TEM, can be viewed as conceptually identical to optical microscopes with electrons replacing photons. Given this analogy the atomic force microscope (AFM) is a touch microscope. The AFM was first demonstrated 25 years ago by Binnig and Quate [49]. Since that time AFM has rapidly become a standard metrological tool. It was originally used to resolve atomic steps on a nearly flat surface.

The performance characteristics of an AFM or other type of scanned probe microscope (SPM) depend intimately on the probe used to interact with the surface. This probe in the analogy used above is the finger with which the surface being scanned is felt. These probes come in many flavors: magnetic, conductive, pyramids with fine points, rods, rods with overhangs, and many more. Each has a different imaging target and performance trade off. While magnetic probes are used for magnetic force microscopy (MFM) and highly conductive probes are used for electrostatic force microscopy (EFM) and other electrically coupled microscopies, the subject of this chapter is the creation of probes based on Si VLS wires for mechanical scanning, that is regular AFM.

The stylus or probe used in Binnig and Quate's original work was a sharp diamond attached to an Au foil. This system was based on tunneling feedback

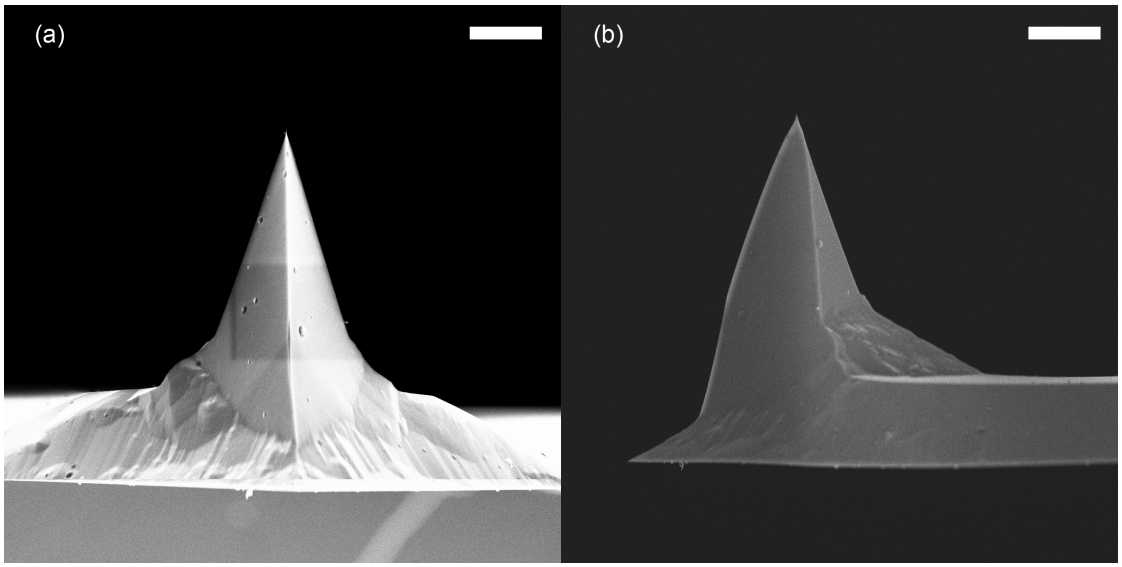

Figure 6.1: SEM images of a TESP AFM probe from the front (a) and side (b). The angles of the tip are 19 degrees sideways, 28 degrees forward and 16 degrees backward. The scale bars are 4 μm.

from a scanning tunneling microscope (STM) tip and operated in what today is known as contact mode. In this mode the probe tip is dragged along the surface of a sample. AFMs were rapidly commercialized and STM based feedback was replaced with optical detection of the probe's height. Along with this, tapping mode was introduced by Digital Instruments in the 1990s [50]. In tapping mode the surface is detected by the reduction in the oscillation amplitude of a vibrating cantilever. This mode of imaging generally outperforms contact mode imaging because the signal is AC allowing the application of narrow bandwidth electronic methods, specifically lock-in approaches for feedback. These provide both sensitivity and noise immunity.

With the commercialization of AFMs mass production of probes was needed. The most common type used to this day is the tapping-mode etched silicon probe (TESP) [51] and similar pyramidal Si probes. An example of a TESP tip is shown in Figure 6.1. These probes offer a fine tip at the end of the pyramid

with a small radius of curvature. This endows these probes with excellent lateral (X-Y) resolution which is determined by the shape of the tip of the probe that actually touches the scanned surface. Combined with AFM's inherently excellent vertical resolution and it would superficially seem such a tip is ideal. For imaging nearly flat surfaces these probes are indeed excellent. However not all features are flat, in this case the half angle of the probe is also important. The angles seen in Figure 6.1 are 28 degrees forward, 16 degrees backward, and 19 degrees sideways. The image formed by an AFM probe and sample ideally is the convolution of the two height profiles (probe and feature), thus these angles appear when the sidewalls angles of features are less than the angle of the probe.

High aspect ratio features are now ubiquitous in both electronics and nano electro-mechanical systems (NEMS). On the micron scale stylus profilometers commonly filled metrological roles measuring the depth of etches and other patterning. On the nanoscale AFM commonly fills this same metrological role. The high aspect ratio features created on the nanoscale both naturally and via lithographically defined means require AFM probes of equal or higher aspect ratios to measure accurately. Although in principle deconvolution is possible with a low aspect ratio probe, in some cases such as a trench a low aspect ratio probe will not physically fit into the desired imaging area. For this reason high aspect ratio probes are employed today in AFM the most common of which are focused ion beam (FIB) milled tips, and carbon nanotube/fiber tips [52]. These probes have high aspect ratios needed but are in general more expensive to create. This is largely due to the need to make the probes individually, although progress has been made at batch fabrication of carbon fiber AFM probes via PECVD growth [53].

Compared with silicon, carbon structures in general are less flexible in terms of subsequent processing. Once grown little structural modification of a carbon fiber or tube is possible besides trimming. Silicon's versatility for structural modification is demonstrated by the entire field of NEMS.

As was demonstrated in chapter 2, it is possible to grow individual Si VLS wires at positions defined by lithography. At large enough diameter these wires will grow with high probability in the <111> direction in the Au-Si and Al-Si systems. In this chapter I exploit these features to create mass producible AFM probes based on Si VLS nanowires.

6.2 Initial concept

The idea of using nanowires as AFM probes was not a new one at the time I began the work described in this chapter. Indeed, Guy Cohen at IBM Research had already patented one concept for the construction of nanowire based AFM tips [54]. While the work described in this chapter was being carried out Engstrom and coworkers demonstrated Si nanowire based AFM probes [55]. What is notably absent in both methods however is site controlled growth of individual nanowires. In the case of Cohen's patent uncontrolled growth is performed and the extra wires are removed. In the case of Engstrom's work the catalyst size is made small in an attempt to grow a single nanowire on a statistical basis. This approach suffers from several problems: it requires expensive high resolution lithography, will not yield wires growing with high probability in the <111> direction, and will have many sites with more than one wire. This last deficiency is clearly seen in Engstrom's paper where even the selected presumably

excellent example of nanowire growth (Engstrom, Figure 4) has two secondary growths near the main tip. These growths are acceptable because they do not interfere with the main tip, however in this process it is likely that many such growths will. From a manufacturing stand point this means that each tip must be inspected with a SEM, a considerable expense.

Before Engstrom's work was published and before I had developed the process allowing site controlled growth of single Au catalyzed Si VLS wires described in chapter 2. Brent Wacaser proposed to create AFM probes from Al catalyzed Si VLS wires. His idea was to use a site controlled growth process developed with Maha Khayyat at IBM Research. In this process a blanket thin film of Al is deposited on a layer of SiO_2 in UHV conditions. This SiO_2 layer has wells defined in it where the bare Si is exposed. Thus the deposited Al film sees two surfaces SiO_2 and clean Si. Aluminum's affinity for oxygen is higher than silicon's. Brent's idea was based on the idea that where the Al touched the SiO_2 it would oxidize by taking oxygen from the SiO_2 and thus not be able to grow a wire. Therefore wires would only grow where the wells were lithographically defined. The wells themselves are defined to be the correct size to on average grow a single nanowire from the blanket deposited film thickness. This method does grow wires at lithographically defined locations but suffers from many of the same issues described for Engstrom's work. Brent did not have time to pursue this idea due to being reassigned to another project inside IBM research and suggested I pursue it.

I decided that it would be better to use Au catalyzed wires using my own site controlled growth methods described in chapter 2. Due to my own inexperience at the time with mechanical devices I consulted with Rob Ilic on AFM cantilever

creation who was helpful and became a collaborator as a result. We decided the most sensible approach would be to simply grow a single Si VLS wire at the end of a flat <111> cantilever constructed from a silicon-on-insulator (SOI) wafer.

6.3 First generation probes

6.3.1 Probe structure and properties

To minimize any possible risk to the nanowire structures in the first generation probes I chose to grow the nanowires as the last step in the AFM probe fabrication process. The fabrication process relies on conventional lithography and micromachining techniques utilizing a SOI wafer with a 5 μm <111> device layer and a 2 μm buried oxide (BOX) layer. No lithographic features smaller than 1 μm are used. The complete fabrication process for these AFM probes can be found in Appendix B. The result of the process prior to wire synthesis is a suspended cantilever with an Au dot in a standard SiO_2 liftoff well (as described in chapter 2). The Au dot is nominally 1 μm in diameter and 50-100 nm thick. By using the site controlled growth process detailed in chapter 2 a single Au catalyzed VLS wire is grown from these Au sites in the <111> direction. Each Au site grows a single wire or no wire. Sites which grow wires can have the wire correctly oriented in the <111> direction or have a kink type defect resulting in a non-vertical wire.

After wire synthesis the probe yield can readily be determined via inspection in an optical microscope. By using the depth of focus of the microscope, correctly oriented wires appear simply as a dot, incorrectly oriented wires ap-

pear as a rod and failed growth sites appear blank. Because probe sorting can be performed optically it should be both rapid and inexpensive to implement.

Using the parameters described the observed site yield for the process is nominally 20% on the SOI wafers. It is likely this can be improved by optimizing the Au thickness, anneal profile, and the reactor parameters of the VLS growth further. Each probe body has 6 cantilevers defined (each with one growth site), resulting in a high probe yield of nominally 74% with the process described. During optical inspection cantilevers which lack useful wires can be removed mechanically.

The nanowire AFM probes may be used with the Au left in place. The Au tip offers a useful biological sensing platform via functionalization using thiol chemistry. Localized thiolates residing at the apex of the nanowire tip would allow interrogation of molecular binding forces and binding events in ambient and fluid environments.

Alternatively the Au can be removed and the wire chemically thinned. Removal of Au is accomplished in a KI/I_2 based Au etch solution. After careful washing to remove residual iodine, the silicon can be oxidized to a desired diameter. The oxide layer can then be removed in a vapor HF chamber. This process increases the aspect ratio of the probes and can create mass producible probes with very large aspect ratios (Figure 6.2). The maximum aspect ratio attainable is determined by the ratio of the vertical and sidewall growth rates in the VLS process. This is determined by the catalyst material and reactor parameters.

The diameter and length of the wire dictate the stiffness of the probe. As-

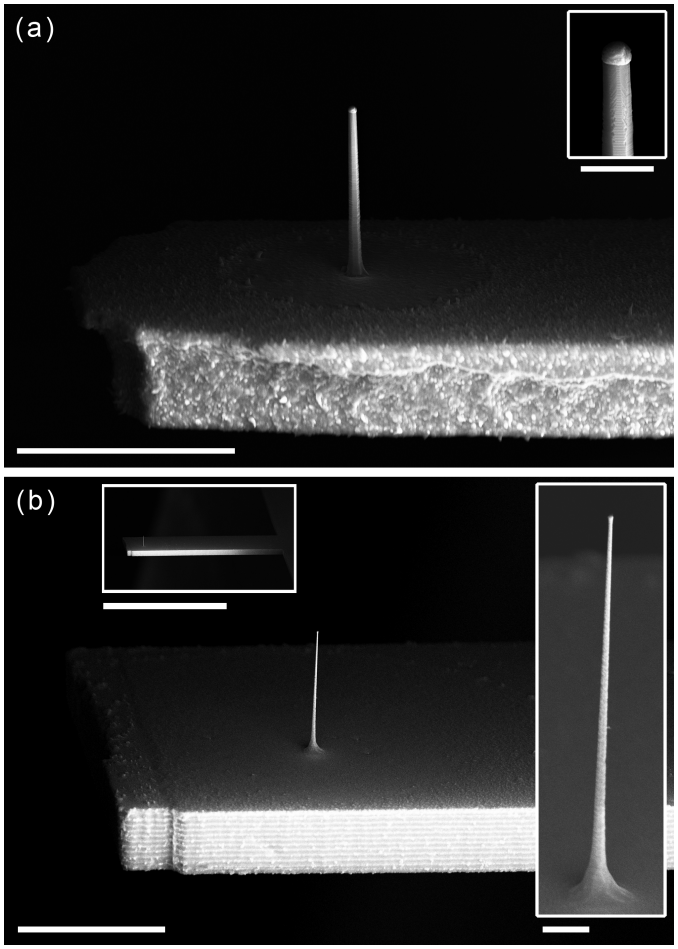

Figure 6.2: (a) A nanowire AFM tip as grown (scale bar: 10 μm). The circular ring around the wire is caused by Au migration onto the bulk surface before the wire is fully catalyzed. This Au changes the morphology of the CVD growth. Inset (scale bar: 1 μm): detail of the nanowire tip as grown showing the faceted single crystal wire and nearly hemispherical Au catalyst tip. (b) An example of a nanowire AFM tip thinned via silicon oxidation (scale bar: 10 μm). The aspect ratio of the tip is 90:1. Inset right (scale bar: 1 μm): detail of the wire after thinning, the slight taper in the wire is carried over from the taper during wire synthesis. Inset top (scale bar: 100 μm): shows the full cantilever AFM probe, the cantilever is 5 μm thick, 125 μm long and 30 μm wide.

suming a cylindrical shape the maximum force that may be applied to a sample via a nanowire probe is given by the Euler buckling force $F_{Euler} = \pi^2 EI/L^2$ where E is Young's modulus, I is the stress moment ($I \approx \pi\frac{r^4}{4}$), and L is the length of the nanowire. This force can be dramatically tuned via the thinning process. Taking Young's modulus to be 185 GPa for a 8 μm long wire the buckling force ranges from 9 nN at r = 25 nm to 11 μN at r = 150 nm.

6.3.2 Probe performance

To assess the performance of the nanowire AFM probes I created a series of trenches in a <100> silicon wafer using 248 nm DUV stepper lithography, a Cl based reactive ion etch (RIE) and an oxide hard mask. The trenches created were nominally 2 μm deep. These trenches were scanned using a Bruker Icon AFM with our experimental AFM probes. In this AFM the mounting angle of the probe is nominally 13 degrees. Because the nanowires are grown normal to the surface this results in the wire being tilted 13 degrees to the surface for scans without rotation.

Performance of a single AFM tip as grown and thinned is shown in Figure 6.3. The fabricated tip diameter combined with the 13 degree tilt limit the trench width that can be probed to 900 nm, with the tip just reaching the bottom of the trench before striking the second sidewall. Thinning the wire via oxidation greatly improves the imaging ability of the tip, allowing both the probing of narrower trenches and the imaging of the flat bottom of the trench. Thinning the wire still further decreases the stiffness ($\propto r^4$) of the probe to the point that imaging becomes difficult. The result is many ringing artifacts while imaging

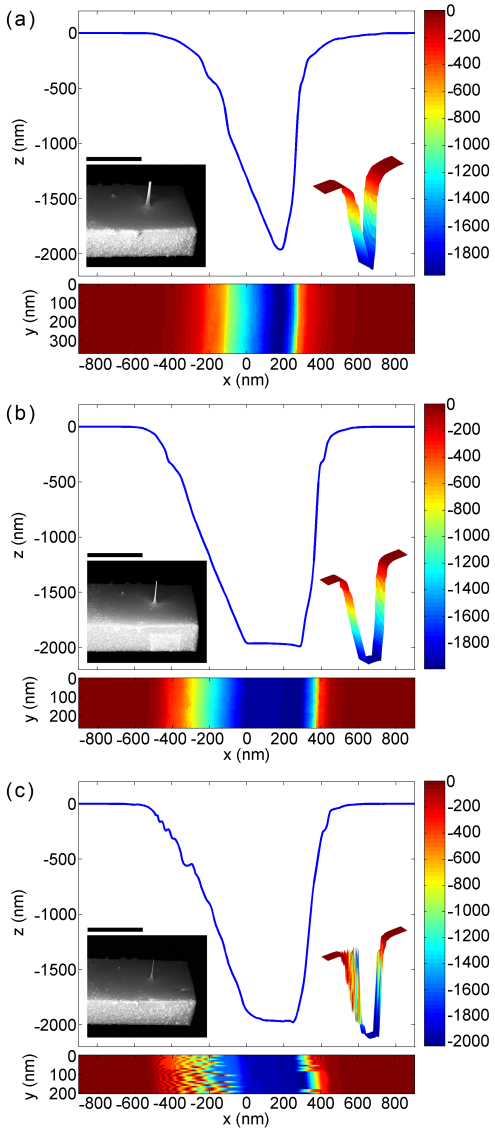

Figure 6.3: Single nanowire AFM tip imaging a 900 nm wide, 1.95 μm deep Cl etched trench during repeated thinning of the tip. The long axis of the cantilever was orthogonal to the long axis of the trenches for the scans. The angle on the negative X-axis is 13 degrees and is caused by the mounting angle of the AFM probe. The depth traces plotted are the mean of the column values in 2D images shown. The insets show the nanowire tip size at the time of scanning (scale: 10 μm). The thinning was performed via oxidation in a dry oxygen atmosphere followed by removal of the oxide in a vapor HF chamber. The as grown diameter of the wire tip (a) when combined with the 13 degree tilt only just allows the wire to reach the bottom of the trench structure. Once the tip is thinned (b) the bottom of the trench is clearly imaged. Thinning the tip further (c) introduces artifacts in the image which cannot be eliminated by tuning the feedback settings of the Bruker Icon AFM used.

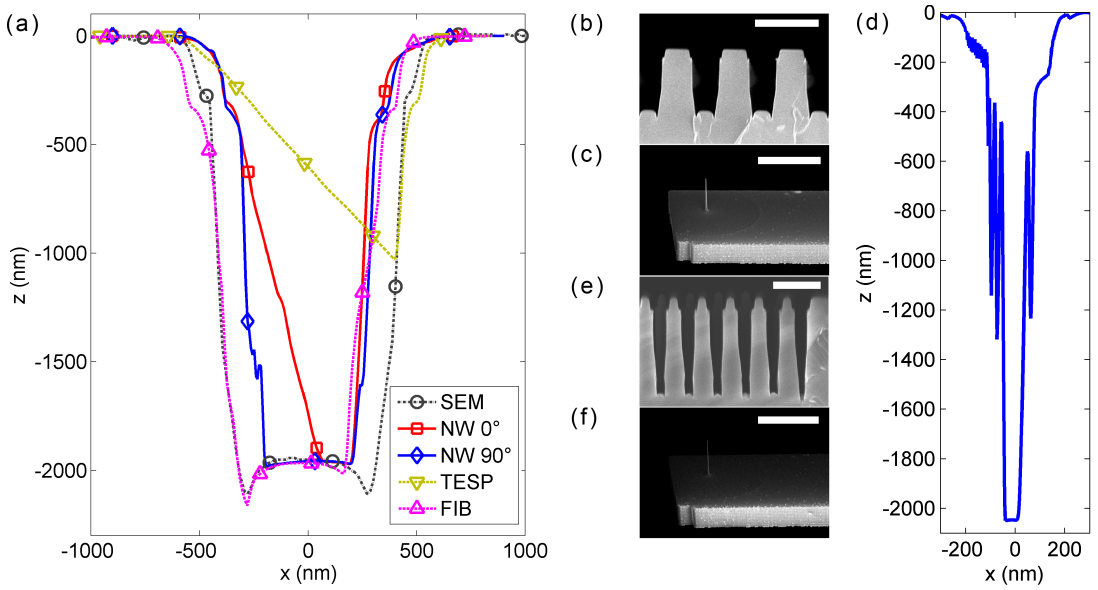

Figure 6.4: (a) The performance of the nanowire tip is compared to a conventional TESP tip and an SEM cross section of the same 1.95 μm deep, 900 nm wide trench. The symbols are plotted every 40th point for the AFM data and every 20th point for the SEM data. The nanowire tip significantly outperforms the TESP tip and agrees very well with the SEM data. The 90 degree image is scanned with the short axis of the cantilever orthogonal to the trench's long axis and the 0 degree image is scanned with the long axis of the cantilever orthogonal to the trench's long axis. The depth traces plotted are averaged by the same procedure as described for Figure 6.3. The encroachment seen at the left and right side of the 0 degree scan from the SEM data is due to the tip diameter at the time of imaging and sidewall interactions. The SEM data shown (a) is calculated from edge of the cross section shown in (b). (c) The tip as used during the scans shown in (a). It is possible to reach the bottom of a 2.05 μm deep, 300 nm wide trench by thinning the nanowire (d), although it does contain ringing artifacts that cannot be suppressed with the feedback settings on the Bruker Icon AFM used. The trenches being imaged in (d) are show in (e). The tip shape at the time of imaging (d) is shown in (f). The scale bars for (b), (c), (e), and (f) are 2 μm, 5 μm, 1 μm, and 5 μm respectively.

(Figure 6.3c). Thinning of a nanowire to this extreme or beyond may still be desirable if X-Y resolution is important, because the diameter of the nanowire tip is the limiting factor of lateral resolution in images without artifacts.

The performance of these nanowire based probes greatly exceeds traditional AFM probes such as the TESP tip for imaging high aspect ratio features and

is similar to commercially available FIB milled AFM tips. Direct comparison of AFM data, taken with the nanowire probes, with SEM cross sections, of the same trenches, shows that the AFM data provides a good representation of the trench structure (Figure 6.4). When scanned at 90 degrees to eliminate the tip's tilt, the only notable differences between SEM and AFM data are a narrowing of the trench due to the diameter of the tip used and the tip's failure to probe the very narrow ion channeling indentions at the well edge again due to the tip's diameter. The performance with rotation approaches that of a commercially available tilt-corrected FIB milled tip. The nanowire probe used in Figure 6.4 was initially 244 nm in diameter. With this diameter trenches as narrow as 500 nm in width could be probed to their full 2 μm depth. By thinning the probe to 84 nm in diameter I probed features as narrow as 300 nm of depth 2.05 μm (Figure 6.4). Although these images contained artifacts they remain useful in cases where well depth is the primary concern and non-destructive probing is required. With an appropriately matched feedback system or a less stiff cantilever it may be possible to reduce or eliminate these stiffness related artifacts. Shortening the nanowire tip to the minimum length needed to probe a desired feature would likely also help remove such effects. It is important to note that the minimum length of the wire depends not only on the feature depth that is to be probed but also on the offset from the front edge of the cantilever and the mounting angle of the probe in the AFM. This offset is required due to alignment tolerances between lithographic layers; its minimum value is set by the tolerances of the lithography I used, and the acceptable reduction in yield due to alignment variation across the wafer. I chose a conservative value to ensure layer to layer alignment was not an issue, but in an optimized process the offset could be reduced.

During imaging I noticed no appreciable degradation in the tip performance. This is reasonable given the flat nature of the tip, nearly uniform diameter of the wire, and relatively low stiffness of the structure. The low stiffness of the probes requires a relatively low tip velocity ($< 0.5\ \mu m/s$) to allow the AFM to track the features; however it also makes the tip fairly resistant to breakage.

These first generation probes demonstrated the possibility of creating wafer scale high aspect ratio AFM probes via a simple process. The high aspect ratios of the probes are fundamentally enabled by the low sidewall taper of Au catalyzed Si VLS wires. The use of Si allows for the application of an extensive existing industrial tool set to modify the resulting probes. Finally the metal tip offers a localize region that can be functionalized selectively with chemistry.

6.4 Second generation probes

6.4.1 Probe structure and properties

The first generation method of creating nanowire based AFM probes is robust and scalable. It creates useful high aspect ratio probes with fairly simple process. The first generation method is not without deficiencies however. In the first generation process lithographic alignment limitations created an offset from the end of the cantilevers which shortens the effective length of the probe, as the diameter of the probe is decreased the stiffness of the wire falls rapidly limiting the minimum lateral resolution or measurable feature size, and the tips are not compensated for the tilt of the AFM probe holder. For high aspect ratio imaging this final drawback is particularly important when imaging

wells which are confined in 2-dimensions. Compensation for tilt is also important from a commercial perspective because existing FIB milled tips offer this feature.

In the second generation process described in this section these issues are removed or mitigated by exploiting the properties of VLS and anisotropic Si etching. The most important new feature of the second generation probe process is the ability to create probes with arbitrary tilt. The key to creating AFM nanowire probes with arbitrary tilt is both the fact that large Si VLS wires grow in the <111> direction and base etches such as KOH etch the <111> direction slowly. By using KOH it is possible to create <111> facets on a Si wafer. By sourcing a wafer cut at a proscribed angle to the <111> surface, the angle to the surface of this facet is defined at the time the wafer is cut and can be chosen arbitrarily. On this facet Au can then be placed and a VLS wire grown. For a large enough diameter it will grow normal to the facet in the <111> direction. With this method one can grow a VLS wire controllably in any direction relative to the top surface of a wafer.

The commercial AFM used for this work as seen in the first generation probes has a mounting angle of 13 degrees. Therefore for this second generation process I wanted wafers with a top surface 13 degrees from <111>. This is not a commonly available crystal orientation so a custom order for these wafers was needed. Even finding a supplier that would create such an arbitrarily cut wafer was somewhat difficult. After sourcing the <111>-13 degree wafers I tested creating <111> facets in the surface with a silicon nitride hard mask and KOH. I determined reasonable parameters for the aperture size and etching time to create 1-3 μm deep faceted wells in the wafers. These tests also allowed the 13

degree angle to be verified and the tilt direction on the wafer measured relative to the wafer flats. After these parameters were determined the next step was to have some of the wafers turned into SOI for use in a new second generation probe fabrication process. I chose to reuse the SOI parameters from the first generation work for these custom SOI wafers save for the change in the device layer orientation. Thus the SOI consisted of a <111>-13 degree 5 μm thick device layer, a 2 μm thick BOX layer and a 500 μm thick <100> handle.

The process for the second generation probes adds the KOH defined well creation steps to that of the first generation. In brief the second generation process consists of 4 major steps. First the facet is defined via KOH etching with a silicon nitride hard mask and the catalyst is placed on that facet. Second the wires are grown via the VLS method. Third the wires are sculpted. Fourth the cantilevers are created and released. The resulting probes are shown in Figure 6.5. Complete details of the second generation process are contained in Appendix B.

As can be seen the facet provides not only the tilt correction needed but also removes the effect of alignment limitations in the lithography. Although the wire grown is still a significant distance from the edges of the cantilever because the facet is parallel to the sample surface at the time of imaging it does not matter where the wire grows within the faceted area and the wire tip can be used to its full length neglecting atmospheric damping effects.

The maximum force that may be applied to a sample via a nanowire probe is given by the Euler buckling force previously mentioned. Because of the strong scaling of this force with wire diameter thinning the probe uniformly using oxidation or other means becomes problematic. This problem can be mitigated

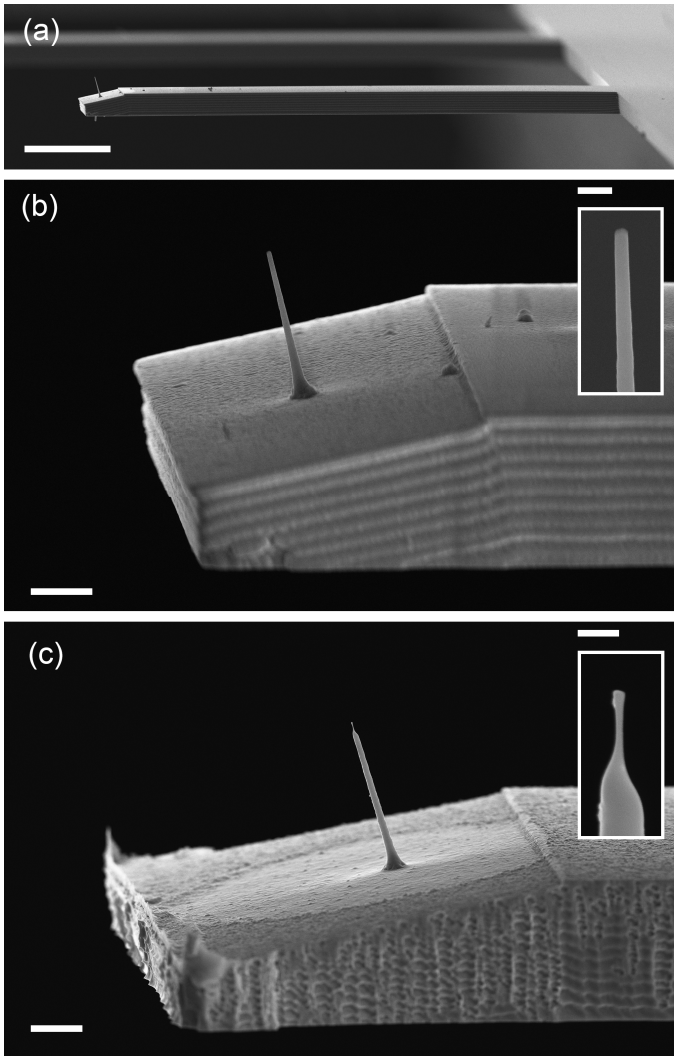

Figure 6.5: (a) A SEM image of a tilt-corrected nanowire AFM tip as grown (scale bar: 20 μm). (b) SEM of the end of the nanowire probe shown in (a) after removal of the Au catalyst showing the KOH defined <111> facet and nanowire tip (scale bar: 2 μm). The inset is a magnified view of the nanowire tip (scale bar: 400 nm). The tip has a width of 153 ± 2 nm and nominal length of 4.7 μm. (c) SEM of the end of a sculpted nanowire AFM probe (scale bar: 2 μm). The inset is a magnified view of the sculpted minor tip (scale bar: 200 nm). The minor tip has a width of 52 nm ± 2 nm and a nominal length of 326 nm.

by two means: making the probe stiffer or by making the cantilever softer. Although simply making thin silicon cantilevers is appealing, it is important to realize that the VLS process that grows the wire also grows background silicon. This silicon has stress and grain structure that cannot be chosen independently of the VLS parameters. Although it could be grown on top of another layer and removed in principle, removing it without removing the wire would be challenging. Thus for very thin silicon this is likely to be a problem for uniform performance.

The alternative is to make the probe stiffer. For successful atmospheric AFM with nanowire probes the probes must provide clearance from the cantilever to reduce the effect of atmospheric damping in tapping mode. This and a desire to probe very deep features both require long wires. In this case uniform thinning will not result in a stiff probe relative to the fixed cantilever stiffness therefore I chose to sculpt the wire to create a step change in the diameter (Figure 6.5c). I call the large diameter section of the wire the major tip and the small diameter section the minor tip. Although the minor tip has a small diameter it remains stiff as it is also much shorter than the major tip. For the tip shown in Figure 6.5c taking Young's modulus to be 185 GPa I estimate the buckling force for the minor tip is 6.1 μN and the major tip is 8.5 μN.

To sculpt the wire and create the minor tip simple bulk processing is used without lithography. After the wire is grown and the catalyst is removed, the wire is oxidized to form a thin layer of SiO_2. After this polysilicon is deposited uniformly on the wafer using bulk LPCVD. Next resist is spun on the wafer to cover the wires completely. After this the resist is plasma etched in SF_6/O_2. As the resist is removed from the tip of the wire the polysilicon is quickly etched

to the SiO_2 layer which serves as a stop etch layer for this process. The length of time of this etch determines the length of the minor tip. The resist can then be removed. At this point the wire has a step change in diameter in it which is approximately maintained during subsequent thermal oxidation. Thus by choosing the thickness of the polysilicon one selects the diameter difference between the major and minor tips (excluding oxidation rate effects of polycrystalline verses single crystal silicon surfaces).

The process outlined above in principle allows for the creation of Si wire AFM probes with arbitrary tilt and lateral resolution. The process needs no lithography smaller than 1 μm, with similar alignment tolerances. In practice there remain stiffness limitations imposed by the chosen device layer thickness, and the fundamental properties of silicon.

6.4.2 Probe performance

To demonstrate the efficacy of these probes I chose to image high aspect ratio trenches and wells as well as MgO particles. The former provide a simple test of the high aspect ratio imaging ability of the probes, while the later allows for assessment of the tilt compensation of the probes.

The MgO particles were deposited on a clean Si wafer by oxidizing Mg ribbon and passing the wafer through the resulting smoke. These MgO particles are cubes (Figure 6.6a inset), which have truly vertical sidewalls and thus allow a direct measure of any tilt in the probe/microscope imaging system. By imaging these particles with the tilt-corrected AFM probe shown in Figure 6.6b we see the probe is well compensated for tilt. Although the imaged sidewall angles

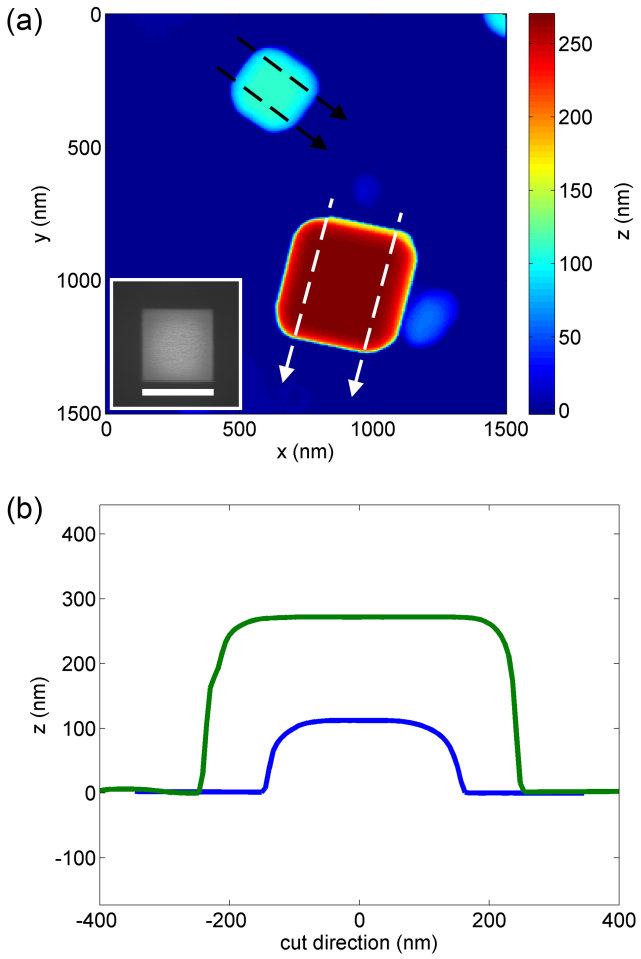

Figure 6.6: (a) An AFM image of two cubic MgO nanoparticles. The height of the smaller particle is 122 nm and the height of the larger particle is 272 nm. The inset SEM shows a typical MgO 302 nm cubic particle (scale bar: 300 nm). The white and black arrows in (a) indicate the direction and integration window for the averaged line cuts shown in (b). The line cuts show a highly symmetric trace with non-zero sidewall angle. The symmetric nature indicates that the probe is properly tilt-compensated, while the non-zero sidewall angle is due to scan quantization and probe interactions with the particle sidewall. The extended width of the traces is likely due primarily to the finite diameter of the probe (shown in Figure 6.5b) and these sidewall interactions rather than non-cubic particles.

are not vertical the trace is highly symmetric. If the probe were tilted it would demonstrate a clear asymmetry. The non-zero sidewall angle in the traces is due both to quantization of the scan and also the probe interacting along its length when the probe is near the faceted sidewall. This interaction also affects the apparent width of the particles in the image. The probe used has a scanning electron microscope (SEM) measured width of 153 ± 2 nm. Taking the particles scanned to be cubes and defining the effective width of the particles to be the distance between the peaks in the derivative of the height data caused by the two edges results in an effective width of the probe of 205 ± 8 nm and 183 ± 8 nm for the large and small particles respectively. These data support probe-sidewall interaction as the cause for the non-vertical sidewalls. Because the probe is parallel to the MgO sidewall facet along its length this interaction is stronger for the larger particle, hence the larger effective probe width and scaling of this width with feature cube height.

To demonstrate a practical use of these AFM probes I imaged features etched into Si wafers using a Cl based reactive ion etch (RIE). The first of these features is shown in Figure 6.7. It is a 600 nm well as defined on the DUV stepper mask. As measured by SEM the transferred well is nominally 588 nm wide at the top and narrows to 395 nm at the bottom. Imaging this structure with a tilt-compensated nanowire AFM probe reveals the well depth after etching is 874 nm. Comparing SEM data of a similar well to the AFM data we see fair agreement by overlaying height contours of −50, −400, and −800 nm (Figure 6.7d). We also see the clear reduction in feature size caused by the finite diameter of the tip (Figure 6.7b). At this depth the strong sidewall interactions cause some ringing in the image not easily removable by adjusting the microscope scan parameters. Although the nominally 6 μm long probe could be used to image a

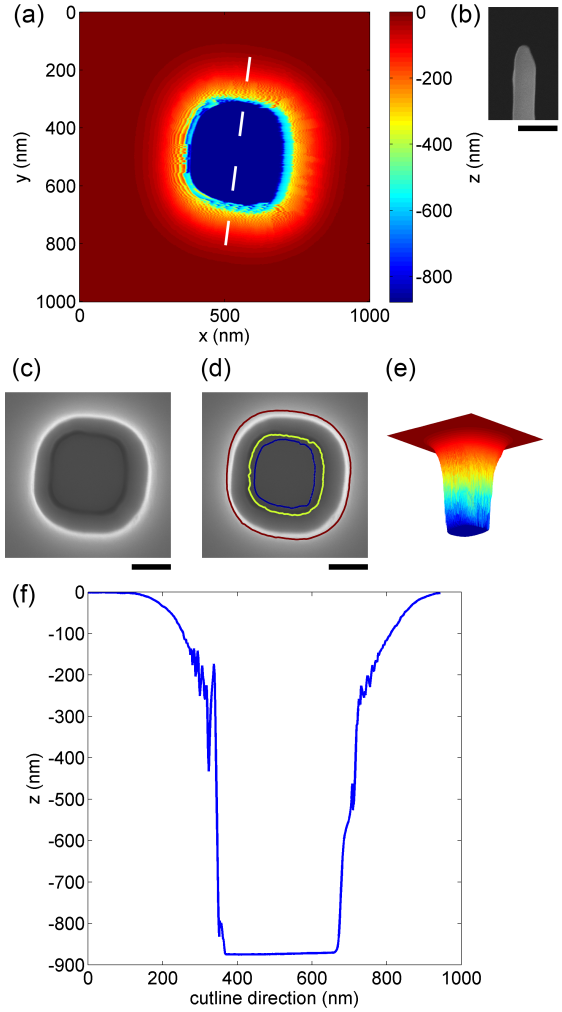

Figure 6.7: (a) An AFM image of a lithographically defined well transferred into SiO_2 hard mask via CHF_3/O_2 RIE and then into Si via a Cl RIE. The image was taken using the probe shown in the SEM image shown in (b) the probe has a diameter of 168 ± 3 nm (scale bar: 300 nm). An SEM of a similar well is shown in (c) (scale bar: 200 nm). The well structure is approximately 588 nm wide at the top and narrows to 395 nm at the bottom. The same SEM data in (c) is shown in (d) with height contours from (a) overlaid. The heights are −50, −400, and −800 nm. The AFM data corresponds to the SEM data well showing effects from the finite probe width in mapping the contours but maintaining the same general shape. (e) Shows the 2D image shown in (a) visualized in 3D with the same extents and color map as used in (a). (f) shows a single line cut across the data in (a) at the position indicated by the white dashed line in (a). It reveals that the well depth after etching is 874 nm. The ringing artifacts are largely the result of tip-sidewall interactions during the scan.

much deeper well these artifacts increase in severity the deeper the feature. A non-atmospheric AFM is likely the best solution to remove these artifacts with this type of probe.

The severity of these artifacts can also be reduced by making the probe stiffer. This results in less bending when the probe interacts with the sidewall of near vertical features. Making the probe stiffer by using a larger diameter tip reduces the effective lateral resolution of the probe. To mitigate this issue I created sculpted AFM probes with a stiff minor tip of small diameter. The minor tip of this type of probe can be tuned for the expected feature dimensions. To test this type of probe I created a pattern of wells, dots and trenches in Si using a Cl RIE combined with electron beam lithography. Hydrogen silsesquioxane (HSQ) was used as the resist/hard mask for the RIE. I imaged this pattern using both a commercially available FIB milled probe (Figure 6.8) and the sculpted nanowire AFM probe seen in Figure 6.5c.

From the resulting images it is clear both the FIB milled probe and the sculpted nanowire probe do a good job imaging the pattern. The difference between the FIB milled probe image and the sculpted nanowire probe image is due to the sharp point on the FIB milled probe. This sharp point allows the FIB milled probe to provide better performance in terms of lateral resolution for features less deep than the sharpen region. However the lateral resolution is a function of depth. In the case of the sculpted nanowire probe the lateral resolution is worse but nearly constant as a function of depth to the length of the secondary/minor tip. Either feature may be desirable. Here the effect is to increase the apparent width of features in the FIB milled probe image relative to the sculpted nanowire probe image. The most demanding feature to image in

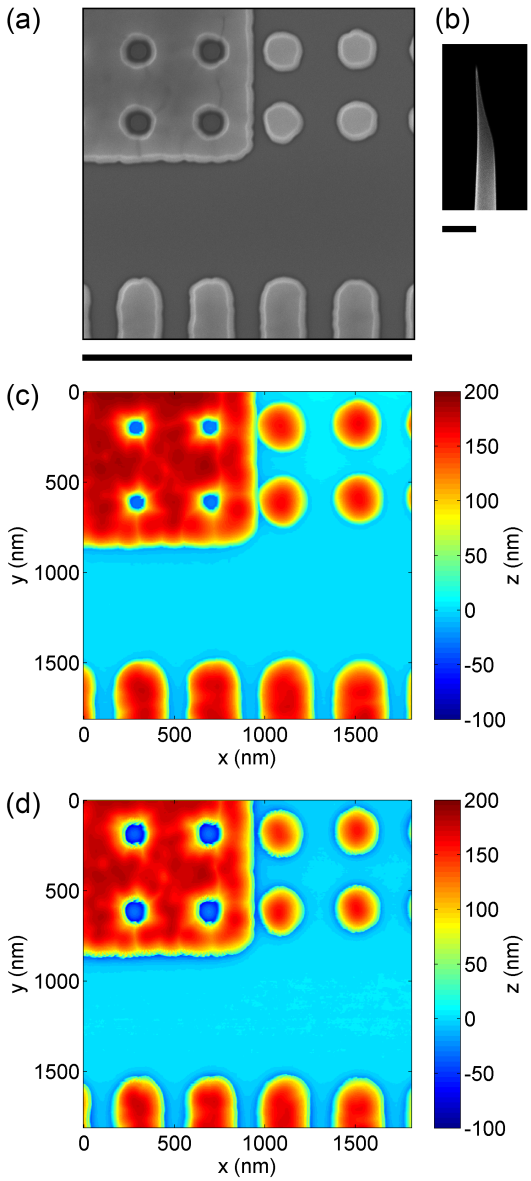

Figure 6.8: (a) A SEM of an electron beam lithography defined pattern transferred into Si using a Cl RIE and HSQ resist (scale bar: 1800 nm). The narrowest features are the circular wells which have a central diameter of nominally 90 nm. The center to center pitch on this pattern is 400 nm. (b) A SEM of the tip of the FIB milled AFM probe used (scale bar: 400 nm). (c) An AFM image of the area shown in (a) using the nanowire AFM probe shown in Figure 6.5c. (d) An AFM image of the area shown in (a) using the FIB milled probe shown in (b). Comparison of the data shows the FIB milled tips sharpened end allows for better lateral resolution for features shallower than the sharpened region. Both probes resolve the pattern well and give comparable metrological height information for non-destructively measuring the depth of these RIE defined features.

the pattern is the small circular wells. The bottom region of these wells is nominally 90 nm in the SEM image (Figure 6.8a). The difference in effective width of the two probes is particularly clear in these circular wells where the nominally 52 nm diameter of the sculpted nanowire probe is significant. However for typical applications such as non-destructively measuring the depth of a RIE etch on a wafer during processing, both probe types are equally effective.

6.5 Summary

VLS grown Si nanowires show clear advantages over traditional top down approaches to creating high aspect ratio AFM probes. These probes have performance that rivals commercial alternatives while offering wafer scale fabrication that FIB milling lacks. By virtue of being made of Si they benefit from the arsenal of industrial tools that are available for standard MEMS/NEMS processing. Leveraging standard Si processing techniques results in probes with tunable properties. Probe yields are high enough to consider commercialization of this approach of creating AFM probes [56].

SPM probes beyond the purely mechanical probes demonstrated in this chapter are also possible. Examples include magnetic force probes using a magnetic catalyst for VLS, molecular force probes using localized thiols on an Au tip, active probes such as a scanned photodiode, microwave probes using a nanowire as a coaxial line and many others. VLS wires unique properties offer many compelling exploitable properties for nanoscopic scanned probe fabrication.

APPENDIX A

FREQUENCY DOMAIN MEASUREMENT OF CARRIER LIFETIMES

A.1 Introduction

For every time domain measurement there is always a frequency domain equivalent. The time domain measurement presented in chapter 5 is conceptually simple. It provides full phase and amplitude information of the transient response of the system via its IQ mixer based detection scheme. These are positive qualities.

However the method used in chapter 5 is not without shortcomings. The principle shortcoming from a practical perspective is probably the cost. The microwave components are not expensive. The detection scheme requires an oscilloscope with 1 GHz or greater bandwidth. Fast oscilloscopes are relatively common today so this is not likely a major issue either. Low phase noise microwave sources and powerful pulsed lasers are both more expensive and less abundant than fast oscilloscopes. Of the two certainly the laser is the most specialized and requires the most care. Even while performing the experiment in chapter 5 the laser would occasionally destabilize. Meanwhile microwave sources are highly reliable test and measurement equipment.

In this appendix I will outline another means by which a lifetime measurement can be made by exploiting frequency domain techniques. This approach removes the need of a high pulse power laser replacing it with a 10 dollar diode laser. This approach does work for low lifetime materials but due to the slow millisecond background decay seen in the VLS data in chapter 5 it does not work

for the VLS materials studied in that chapter. I am documenting the approach in the event any reader might find it a more practical means for measuring a low lifetime sample.

A.2 Concept

The time domain detector used in chapter 5 was basically a ultra-wide bandwidth AM direct conversion receiver. It was a very wide dynamic range instrument as well in terms of the injection levels it could measure. However this function was largely provided by the compression of the voltage amplitude by the sample configuration. In general one of the major advantages of frequency domain methods are the very large dynamic ranges and low noise floors they enable. These benefits are largely derived from high Q filters, a type of gain bandwidth product trade-off.

Although it would be possible in principle to use a triggered spectrum analyzer in place of the mixer in the time domain measurement, the method used in chapter 5 makes more sense if a low duty cycle pulse laser is to be used. However when I considered the idea of using a spectrum analyzer to increase the sensitivity of the measurement in chapter 5 my mind was opened to the idea of changing the stimulus as well.

If the sample were a tuning fork the method in chapter 5 would be hitting it against a hard object and listening to it ring. An alternative to this would be to play tones near the tuning fork and observe when it starts to vibrate.

If you shine a light on a semiconductor you will generate excess carriers

in it beyond the population in thermal equilibrium. The number that exists in excess depends on two rates, the rate of carrier generation and the rate of carrier recombination. The first is proportional to the light intensity the second is what we wish to measure.

If a light is on in steady state then this out of equilibrium density is also steady. In the quasi-static limit of varying the light intensity the same idea will apply. Essentially the excess carrier density will just be instantaneously proportional to the light intensity. If the light intensity is modulated much faster than recombination can occur however the carrier density will not be able to track the light intensity.

This effect can be put to use by measuring the reflected (or transmitted) microwave power in response to a sinusoidally modulated laser. If the system has only a simple first order recombination process then this response will look like a low pass filter, the pole of the response indicating the lifetime.

This method is powerful in that all systems will look approximately first order at very low injection levels. The low noise floor of the measurement operating in the frequency domain enables detection of very small conductivity changes assuring this condition.

A.3 Experimental setup

In the simplest form this method requires only a microwave source, a means of separating out the input and output signals such as a directional coupler, an antenna or means of coupling the microwaves to a sample and a modulated

laser capable of frequencies above the expected lifetime of the sample.

In practice other components may be useful given available equipment. A schematic showing one implementation of this scheme is shown in Figure A.1. Amplifier selection largely drove the configuration shown as the expected signal size was below the noise floor of the spectrum analyzer without amplification. However some spectrum analyzers will have built in preamps for this purpose so many of these additional filters and mixers could be eliminated in many versions of this measurement.

The laser chosen for this setup was a 850 nm 2.5 GBPS laser designed for fiber Ethernet. Being a commodity part it only cost about 10 dollars. To get reasonable data the flatness of all components in this measurement needs to be accounted for as best as possible and removed numerically from the resulting data.

One additional benefit of using a frequency domain method over a time domain method is not only the Q of the receiver but also that the sample can be in principle placed in a cavity, the Q of which can act as gain for the measurement.

Conceptually in this experiment the laser tone AM modulates the microwave carrier tone reflected from the sample. This creates sidebands on that carrier tone in the spectrum. By measuring the amplitude of those sidebands as a function of the laser modulation frequency the low pass response can be measured.

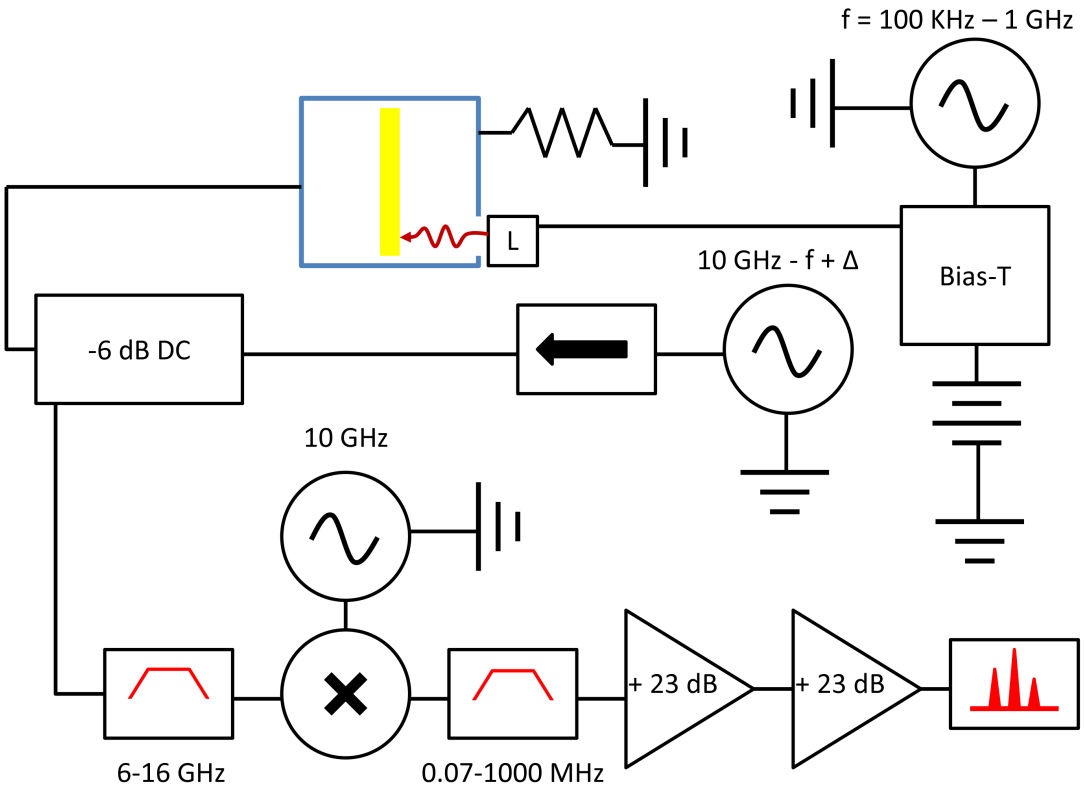

Figure A.1: One implementation of the frequency domain method is illustrated in this block diagram. The sample shown in yellow is mounted inside two WR90 waveguide couplers the second of which is terminated with a 50 ohm load. These coupliers form a cavity shown in blue for the sample under study. One coupler has a hole drilled in it to allow a small 850 nm 2.5 GPBS laser diode (L) inside the cavity. This laser is driven with a sine modulation at frequency f. A microwave tone is applied to the sample after passing through a ferite isolator and directional coupler at a frequency of 10 GHz $- f + \Delta$. The light modulating the sample conductivity produces a sideband on this carrier frequency that is always at 10 GHz + Δ. This signal is separated by the directional couplier, passed through a filter, then downmixed by a double balanced mixer. Finally the signal is again filtered and amplified before being measured via a spectrum analyzer. The use of two microwave sources and the mixer enable the sideband to always be at the same frequency minimizing the leveling considerations for the amplifiers and analyzer.

A.4 Example data

As always it is best to test a design on something simple first before applying it to something difficult. To do this I chose to measure the lifetime of a chip of semi-insulating GaAs. The result of this measurement is shown in Figure A.2. As can be seen the data is a fairly good fit to a simple low pass response. The deviations present are all likely due to calibration and leveling issues. The lifetime is easy to extract from the data and is about 5 ns. The increased spread of the data as it reaches near −20 dB in the plot is due to reaching the noise floor of the setup. The disagreement at low frequencies is likely a leveling issue, in the calibration.

Clearly this method is able to resolve very short lifetimes very well and with less expense than the time domain method. Applying it to VLS materials however did not work due to the slow decay process present in parallel with the fast process. If you consider the power in each signal in the time domain it is clear that the slow signal has more energy. This results in it covering up the fast signal in frequency domain to the resolution of this measurement. For samples without this feature the frequency domain method of this appendix should work well.

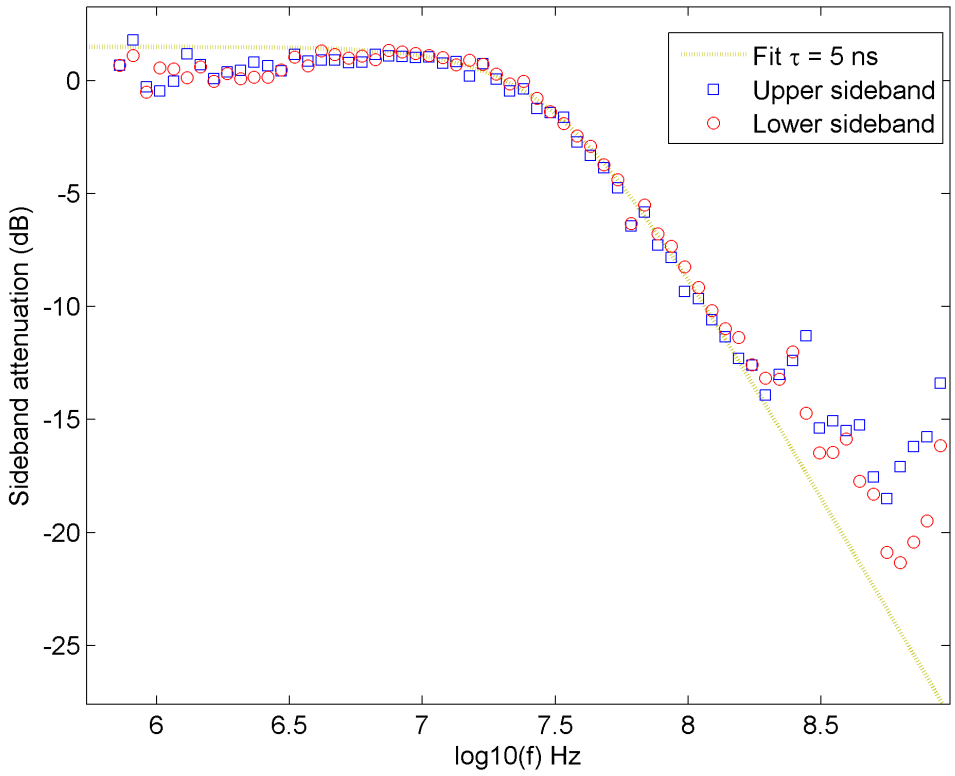

Figure A.2: Shown are the relative magnitude of the sidebands created via the frequency domain setup shown in Figure A.1. Both the upper and lower sidebands are measured. The data is fit to a first order low pass response with a time constant of 5 ns.

APPENDIX B

NANOWIRE ATOMIC FORCE MICROSCOPY PROBE FABRICATION METHODS

B.1 First generation probe fabrication process

Fabrication of silicon the first generation nanowire AFM probes proceeds from a silicon-on-insulator (SOI) wafer consisting of a 5 μm <111> device layer and a 2 μm buried oxide layer (BOX).

The wafer is RCA cleaned and loaded into a wet oxygen environment oxidizing the wafer to nominally 150 nm. The wafer is then removed and placed in a plasma enhanced chemical vapor deposition (PECVD) chamber where nominally 3 μm of SiO_2 are deposited on the back side of the wafer (Figure B.1a).

The wafer is then coated in SPR-220 resist and contact photolithography is performed defining alignment keys (marks) on the front side of the wafer. These keys are transferred into the wafer using reactive ion etching (RIE). First the oxide layer is cleared using a CHF_3/O_2 etch, then the keys are transferred into the silicon layer using a Bosch etch. The resist is then removed in organic solvents.

The backside of the wafer is coated in SPR-220 resist and contact lithography is performed defining windows around the body of each AFM probe (Figure B.2b). These windows amount to the negative body of the AFM probes inside a bounding box. This pattern is transferred through the thick PECVD oxide on the backside of the wafer using a CHF_3/O_2 RIE. Alternatively hydrofluoric acid (HF) can be used to clear the back oxide layer. Following this the resist is removed in organic solvents.

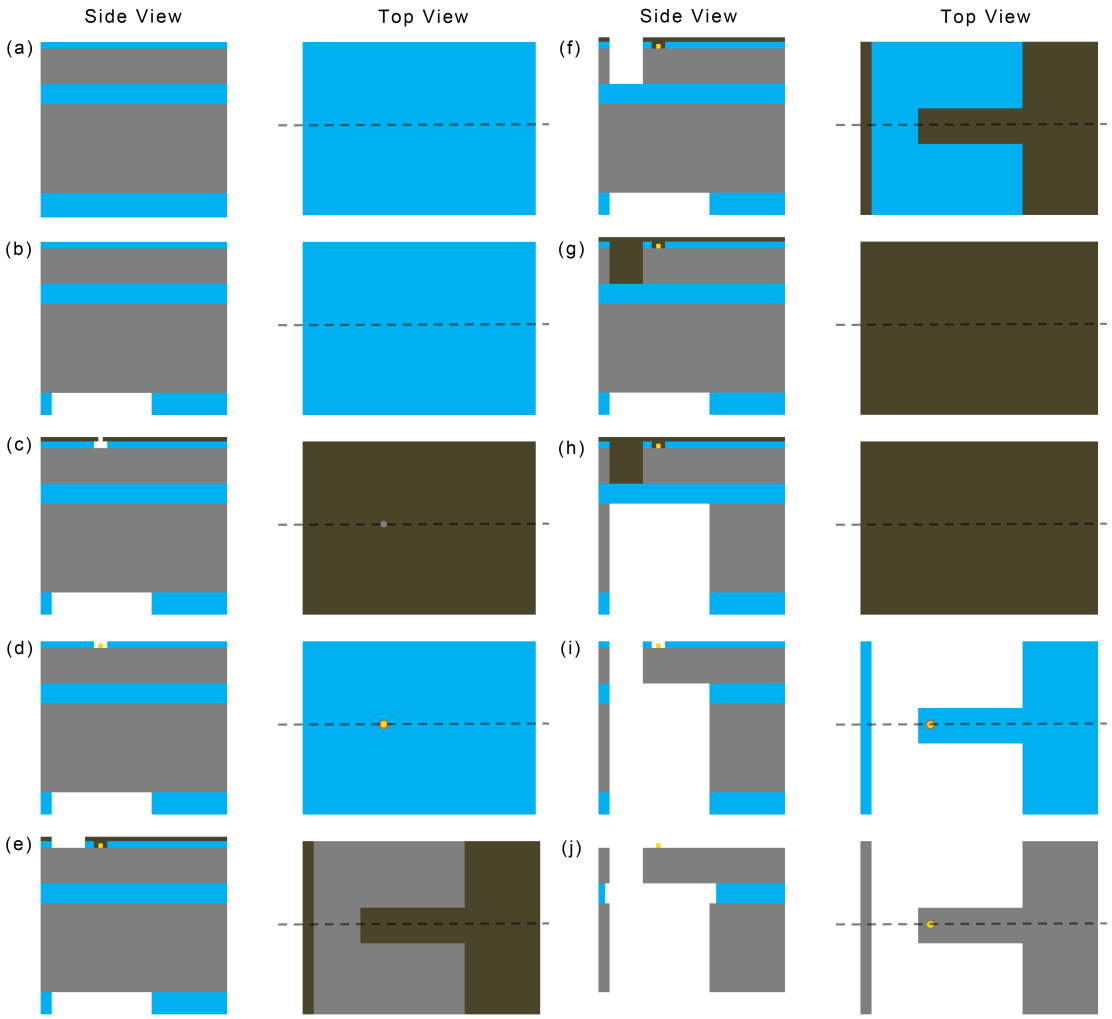

Figure B.1: Schematic representation of the process flow for AFM probe fabrication (not to scale). In the figures blue is SiO2, gray is Si, Gold is Au, and tan is resist. After the creation of the main layer stack (a), the backside window is defined (b), the nanowire catalyst site is defined (c), Au is evaporated and lifted off (d), the cantilevers are defined in the device layer (e) and (f), and the cantilevers are released (h) and (i). Finally the top oxide is stripped just before wire growth (not shown). After growth the probe is then complete and can be used.

The front side of the wafer is then coated in SPR-200 resist and the cantilever pattern is defined using contact lithography. This pattern is transferred only half way through the oxide layer. This allows the alignment of the next step to be checked locally to ensure there are no gross errors. This step would not be needed for mass production. The resist is then removed in organic solvents.

The front side of the wafer is coated in SPR-700 resist. 1 μm dots are defined at the tip of each cantilever using an i-line stepper. The pattern alignment can be optically checked locally to the cantilever pattern assuming the prior step is carried out, otherwise it can be difficult to find the pattern. This pattern is transferred half way through the oxide layer using a CF_4 RIE. The remainder of the oxide layer is cleared in a buffered oxide etch (BOE) 30:1 solution. A 100:1 HF solution is then used followed by a DI rinse. This leaves a pristine hydrogen terminated silicon surface under and undercut SPR-700 liftoff mask (Figure B.1c).

The wafer is immediately loaded into an evaporation chamber after being dried with N2. The chamber is pumped to a pressure less than 2x10-6 Torr and Au is evaporated at a rate of 2-3 /s to a thickness of 50-100 nm. The wafer is removed from the chamber and liftoff is performed in N-Methyl-2-pyrrolidone (NMP). This leaves a 1 μm Au dot inside a larger SiO_2 well (Figure B.1d).

SPR-220 is then spun on the front side of the wafer and the cantilever pattern is defined using contact lithography. The resist is baked overnight in an oven at 90 C. The pattern is transferred fully through the oxide layer (Figure B.1e). The pattern is then transferred through the device layer using a Bosch etch. This etching stops on the BOX layer (Figure B.1f).

Following this step the side of the 150 nm front side oxide is exposed. To cover this layer SPR-220 is again spun on the front side without removing the previous resist layer. In order to ensure the solvent is removed from the film, the resist is baked overnight in an oven at 90 C (Figure B.1g). Residual solvent during one of the subsequent deep silicon RIE steps will cause the resist film to bubble thereby compromising the etch masking of the resist.

The wafer is then placed with face down in a Bosch etcher and the body of the probes are transferred using the oxide mask defined earlier (Figure B.1h). This etching stops on the BOX layer. The front side resist provides further mechanical support to the thin BOX layer during this step.

The wafer is then placed in HF and the BOX layer is removed. Following this the resist is removed in organic solvents. This results in a released cantilever structure with Au dots inside oxide wells (Figure B.1i).

These oxide wells can be used to confine Au migration if desired. However if Au comes in contact with a thick oxide layer it can be pinned at the contact point. This can lead to undesirable kinking effects that will cause wires to not grow vertically. At typical temperatures used in SiH_4 reactors this oxide layer is not essential and yield of vertical wires can be better without it particularly in the case of large arrays of wires. Annealing at high temperatures or for long times can also improve vertical yield.

For the wires grown in these experiments we choose to completely strip the oxide layer in HF prior to wire synthesis. This is done in an HF 10:1 solution. This leaves an isolated Au dot on a hydrophobic Si surface (Figure B.1j).

After the HF step the wafer is immediately loaded into a turbo pumped load-

lock. Once the loadlock is pumped the wafer is transferred into a main chamber of a UHV CVD reactor. The temperature of the main chamber is 600 C. The sample is allowed to equilibrate and anneal in UHV for 5 minutes at which point pure SiH_4 is flowed. The chamber is pressurized to 250 mTorr. In this atmosphere the wires nucleate and grow. The time determines the wire length. A typical growth time is 10-30 minutes.

The wafer is then removed from the chamber into the loadlock and cooled under vacuum. After this the probes may be broken out and used or thinning if desired. The nominal diameter of a nanowire grown by the process described is natively 250-400 nm.

To thin a probe the Au tip should first be removed. To do this the sample is dipped in HF to remove any oxide over-layers then carefully rinsed in DI water. Following this the Au is removed in KI/I_2 solution, rinsed in DI then HCl then DI. It is essential to completely remove all iodine from the sample before oxidation as it greatly enhances oxidation of silicon.

The sample can then be oxidized in a dry or wet oxygen furnace. This oxide layer can then be removed using a vapor HF chamber. The diameter of the resulting AFM tip is governed by the oxidation thickness and the initial wire diameter.

B.2 Second generation probe fabrication process

Here I outline my method to fabricate vapor-liquid-solid (VLS) nanowire atomic force microscopy (AFM) probes with arbitrary tilt, diameter and length. The

process consists of 4 main procedural sections: (A) definition of a <111> facet on a silicon on insulator (SOI) wafer and placement of catalytic Au particle on the facet, (B) growth of a Si VLS nanowire from the Au particle, (C) probe sculpting, (D) fabrication of the AFM cantilever.

If only simple uniform thinning of the wire is needed the probes may be fabricated with an order of ADBC. This order is similar to the first generation fabrication process. By placing the wire growth after the complete fabrication of the AFM cantilever there are many fewer steps in which the wires may be damaged. However this ordering is less flexible for creating nanowire AFM probes with minor tips (secondary sections with small diameters). Therefore here I describe the procedure used to create the probes seen in the chapter 6 for the tilt-compensated probes with a minor tip which is conceptually ABCDC.

The process flow for sections A, B and D is illustrated schematically in Figure B.2. The process for section C is seen more clearly via SEMs which are reference inline in the description which follows.

Large Si nanowire in the Au-Si system grow strongly in the <111> direction. KOH and other base etches etch this direction slowly. Therefore it is possible to create <111> facets in a wafer simply by masking the surface of the wafer and placing the wafer in hot KOH. For this work I wanted to create probes which were compensated for the 13 degree tilt of common commercial AFMs. To do this I sourced a SOI wafer with a <111>-13 degree device layer that was 5 μm thick. Below this the SOI wafer had a 2 μm BOX layer that serves as an etch stop and a <100> handle. The orientation of the handle is largely a matter of availability or taste. I chose <100> to break the wafer into rectangular pieces easier after fabrication. This type of SOI was not readily available so we had it

produced for this work to my specification.

To define the <111> facets on the wafer I first deposited low stress low pressure chemical vapor deposition (LPCVD) nitride on the SOI wafers. I then defined both alignment keys and the facet wells using an i-line stepper and SPR-700 resist. This pattern was transferred through the Si nitride using a CF_4 reactive ion etch (RIE). After this the resist was removed and the wafer placed in 25% solution of KOH and water at 75 C for 8 minutes (Figure B.3a). The wafer was then cleaned via an RCA clean, and the nitride removed using hot phosphoric acid. Following this the wafer is again RCA cleaned and oxidized in a wet oxygen atmosphere at 950 C for 30 minutes to create a nominally 200 nm thick SiO_2 layer. After this an additional 3 μm of plasma enhanced CVD (PECVD) oxide is deposited on the backside of the wafer.

The next step is to create the windows in this thick back side oxide. This is done using SPR220 resist with a 7 μm thickness and contact lithography aligned to the front side. The pattern is transferred into the oxide layer using CHF_3/O_2 RIE. Once the pattern is transferred the resist is stripped and the wafer again RCA cleaned.

Low stress LPCVD silicon nitride is again deposited on the wafer to a nominal thickness of 30 nm. The wafer is then placed in a CF_4 RIE to remove this nitride layer from the front side of the wafer only. The purpose of this thin nitride layer on the back of the wafer is to protect the oxide layer from hydrofluoric acid (HF) which will be used later.

At this point the wafer consists of a 200 nm thermal oxide on the front side of the wafer coating alignment marks and <111> faceted wells. On the back side

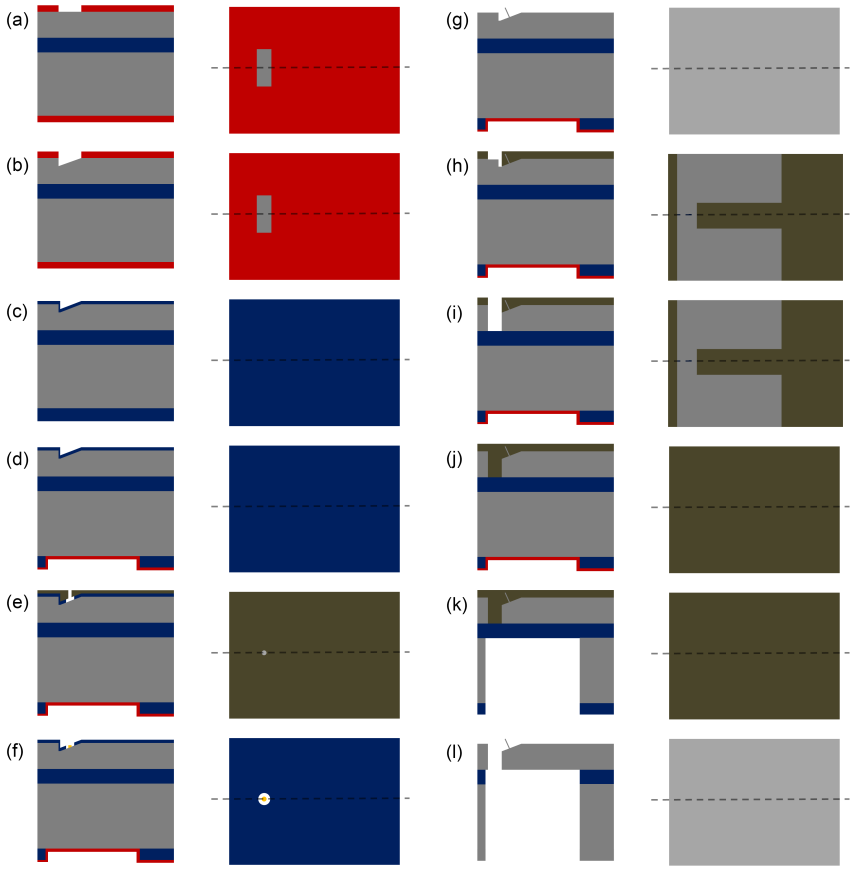

Figure B.2: A schematic representation of the process flow for making a tilt-compensated nanowire AFM probe excluding the probe sculpting steps which occur after step (g). (a) A SOI wafer with a <111>-13 degree 5 μm thick handle, 2 μm thick BOX and <100> handle has silicon nitride deposited on it and a lithographically defined window etch via CF_4 RIE. (b) The nitride serves as an etch mask to create a <111> faceted well at 13 degree to the surface. (c) The wafer is oxidized thermally and PECVD oxide is deposited on the back side. (d) A lithographically defined window is etched in the back of the wafer via CHF_3/O_2 RIE defining the body of the probe. (e) Stepper lithography is performed to etch a nominally 1 μm well into the top thermal oxide. The etch is made via a combination of CF_4 RIE and HF with the HF providing undercut. (f) Au is deposited into the well via electron beam evaporation and liftoff of the resist. (g) VLS grow is performed forming a nanowire. This wire has the Au tip removed and is sculpted various methods. (h) The cantilevers are defined lithographically. (i) The lithography is transferred into the device layer to the BOX via a Bosch RIE. (j) The nanowire is protected via a hard baked resist layer spun on the front side of the wafer. (k) Bosch RIE in conjunction with the back side oxide hard mask is used to etch to the BOX layer from the back. (l) The resist is removed in organic solvents and the oxide is removed in HF releasing the cantilever.

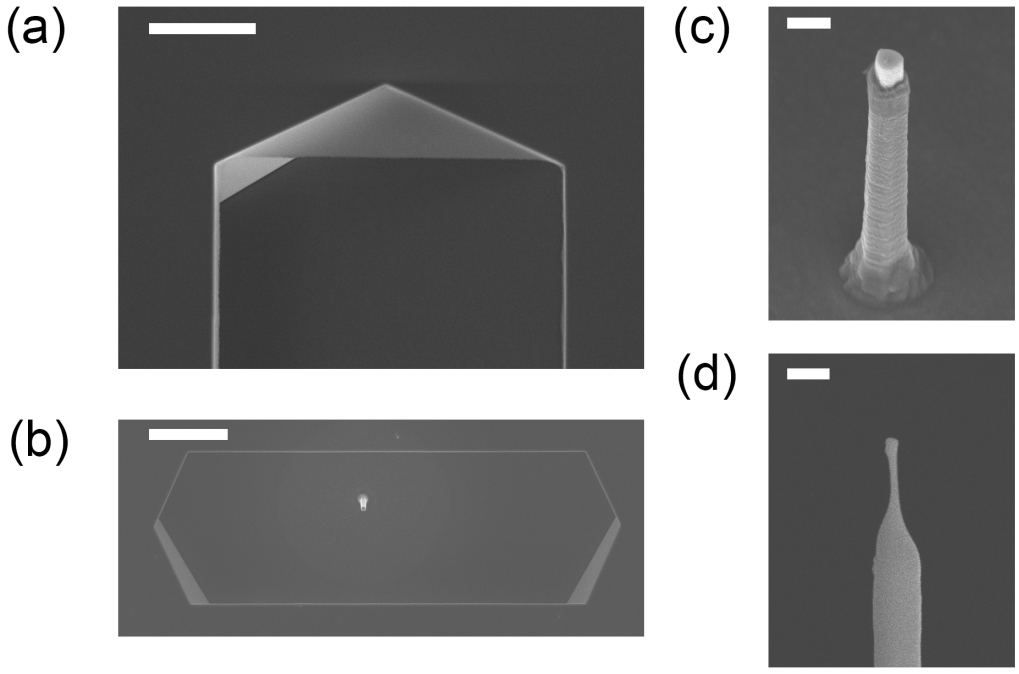

Figure B.3: (a) A SEM showing a KOH etched well with nitride membrane. The bottom surface of the well is a <111> plane at 13 degrees to the top surface (scale bar: 8 μm). (b) A SEM showing a single Au catalyzed Si nanowire growing in the <111> direction in a KOH etched well (scale bar: 8 μm). (c) A SEM showing a VLS Si nanowire with thin thermal oxide surrounded by polysilicon which has been removed from the tip of the wire via an SF_6/O_2 RIE (scale bar: 800 nm). (d) A SEM showing a tip similar to that in (c) after uniform oxidation and removal of the oxide in HF.

the wafer has a pattern in 3 μm thick oxide that will define the edges of the body of the probe. This pattern is capped in silicon nitride.

SPR220 resist with thickness 3 μm is then spun on the front of the wafer and used in conjunction with an i-line stepper to define nominally 1 m circles centered in the <111> faceted wells. This pattern is transferred into the top oxide layer using a CF_4 RIE to a depth of half the oxide thickness. The wafer is then placed in buffered HF (30:1) for 24 minutes. This clears the well to the Si

surface and provides an undercut under the resist. The wafer is then washed in deionized water (DI), dried and immediately loaded into an electron beam evaporator where Au is deposited to a thickness of 80 nm at a pressure less than 2 μTorr.

The next step to create the probes is to grow the VLS nanowires. First the front oxide is removed in 10:1 HF. The wafer is then loaded immediately into an ultra-high vacuum (UHV) CVD chamber. Once under vacuum the wafer is annealed at 600 C for 5 minutes to allow the Au to form a hemisphere, then SiH_4 is turned on pressurizing the chamber to a pressure of 250 mTorr. The time of this step determines the wire length. For the second generation probes used in chapter 6 the growth time was nominally 25 minutes (Figure B.3b).

After growth the next step is to shape or sculpt the wire tips. To do this first the Au must be removed. This is done in KI/I_2 based Au etch. First the wafer is placed in HF, to remove overlayers of oxide, then it is cleaned in DI, then it is etched in KI/I_2, then it is cleaned in DI. This process is repeated twice remaining each time in the Au etch for long enough to remove all of the Au at the manufacture specified etch rate.

The tip can now be thinned uniformly via oxidation. Alternatively a secondary or minor tip can be formed out of the top section of the nanowire by the following means. First the wafer is oxidized at 900 C in a dry oxygen atmosphere for 30 minutes to form a stop etch oxide layer. Then polysilicon is deposited in an LPCVD reactor at 620 C for 11 minutes at a pressure of 150 mTorr. This creates a conformal nominally 100 nm thick layer on the wire, which increases the diameter of the wire by 200 nm. This layer thickness determines the diameter difference in the major and minor tips.

To create the step change in the diameter resist is spun carefully on top of the wires. The resist can either be much thicker than the wire heights or one can rely on the viscosity of the resist to coat the wire sidewalls. Either way the resist should be ashed to expose the top of the wire to a desired length so that the polysilcion can be removed to the stop etch oxide layer. Using SPR-220 with a 3 μm thickness I found the simplest means was to combine the ashing and polysilicon etching steps using a timed single SF6/O2 etch for both. This etch is highly selective to oxide and so terminates radially to produce the desired step change in the wire diameter (Figure B.3c).

Following the etch the resist is removed and the wire oxidized through the polysilicon layer. This combines the stop etch oxide layer and the oxide forming from the polysilicon into a single oxide layer. For the probes used in the main paper this oxidation was performed in a dry oxygen atmosphere for 200 minutes at 1075 C. This oxide layer is then removed in HF (Figure B.3d).

At this point the probe tips have the desired diameter change and length. The final steps create and release the Si cantilever. To do this resist (SPR-220 to a thickness of 7 μm) is again spun on the front side of the wafer and patterned with an i-line stepper. Although this resist greatly exceeds the depth of focus of the stepper the front side cantilever pattern has no small features, and thus is writable with a high enough exposure dose. The 7 μm thickness of the resist completely covers the nanowire tips.

This resist pattern is transferred through the device layer to the BOX layer using a Bosch process based RIE. The resist is then removed and recoated uniformly on the front side of the wafer and baked in an atmospheric oven at 90 C for at least 24 hours to removal all of the solvent. This resist layer protects the

nanowire tips during the back side through etch which is the next step. This through etch is carried out using the back side oxide pattern previously defined and is transferred to the BOX layer using the same Bosch based RIE tool. The front side resist is then removed in organic solvents. Finally the BOX layer is removed in HF. This completes the release of the AFM cantilever. The probes are now usable in an AFM. If desired additional uniform thinning can be performed using oxidation and vapor HF etching. If the polysilicon thickness is picked aggressively this step is not needed, however for the conservative 100 nm thickness I chose it was needed to produce the nominally 50 nm minor tip used for comparison to the FIB milled tip in chapter 6.

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